Digital Single Market

Projects story26 October 2011

Microchips for the mobile information age

The latest microchip technology developed by EU-funded scientists could enhance future generations of processors, in particular those used in mobile devices like tablets and smart phones which are leading the way to the mobile information age.

 [1]

Last year, sales of smart phones exceeded laptops for the first time, indicating that we are well into a new phase of the information age. Call it the mobile information age!

During the initial phase of the internet age, desktop personal computers and later laptop computers were connected together as well as to information sources via telephone land lines in buildings. In this early information age, some people were connected to the internet quite often, many only occasionally and most almost never.

This has changed rapidly with the development of wireless communications, ultimately leading to smart phones that are always connected. All this is possible thanks to powerful electronics that are lighter and more compact, yet perform faster and better.

But emerging devices and services will require a new generation of smaller, low-energy microchips that offer higher data rates, and the European Union is investing heavily in state-of-the-art technology to ensure the continent maintains its leading role in the information society. And the 'Dual-channel CMOS for sub-22 nm high performance logic' [2] (Duallogic) project is an example of this pan-European effort.

'We sought to give a performance boost to future devices operating at lower power supply voltages, so you would get more performance for less energy. This is required for the kind of multimedia applications that run on small handheld devices powered by limited batteries,' says Athanasios Dimoulas, coordinator of the Duallogic project, which received EUR 5.8 million of its EUR 9.3 million

budget from the European Union.

Performance and low-power operation were the two goals of the project - a highly ambitious Seventh Framework Programme [3] STREP project. After 40 years of continuous miniaturisation, further boosting microchip performance has become an increasingly difficult challenge.

So the scientists, engineers and designers at Duallogic had to get creative. They kept silicon as the substrate but looked beyond silicon to less common semiconductor materials to create the conduction channel inside the millions of transistors making up a microchip.

By exploiting the unique properties of a variety of semiconductor materials, the Duallogic team hoped to push the performance of microchip circuits beyond the limits intrinsic to silicon, paving the way for more efficient circuits and smaller scales.

'It is widely known that an integrated circuit - the "brain" of all electronic systems - is made of silicon. While this material is abundant in nature and easy to work with, it does not allow electrons to run through it as fast as we would like, particularly in low voltage applications,' notes Dr Dimoulas.

'In the Duallogic project, we wanted to replace [the] silicon channels of transistors with higher-mobility semiconductor materials like germanium and compound semiconductors to make the charge carriers - electrons and holes - move faster through the transistor.'

It was very challenging because the team worked on large-scale silicon wafers using industrial-scale techniques. This is why Duallogic included so many of the continent's leading institutes and industrial players, such as Belgium's imec and Katholieke Universiteit Leuven, AIXTRON in Germany, CEA-LETI and STMicroelectronics in France, NCSR DEMOKRITOS in Greece, Glasgow University in the UK, and IBM-Zurich in Switzerland.

Twice the logic

The project was called Duallogic because it used different channel materials for each of the two transistors found on microchips, the positive p-type and the negative n-type. The team chose Germanium (Ge) and SiliconGermanium (SiGe) for the p-type transistors and IndiumGalliumArsenide (InGaAs), a compound semiconductor, as a promising candidate for the n-type transistor. The materials were chosen because they offer high mobility for the charge carriers in each type of transistor.

The InGaAs compound is known as a III-V semiconductor, so-called because it is composed of elements from the third and the fifth columns of the periodic table. These compounds offer much higher mobility, a measure of how easily charge carriers can move about inside the semiconductor lattice. Greater mobility ultimately leads to higher performance. Likewise, Germanium offers higher mobility for p-type transistors.

'This approach is considered to be high on the priority list for many RTD and technology integrator labs around the world,' notes Dr Dimoulas. It has proved a very successful research path for the Duallogic consortium, too. 'We successfully integrated SiliconGermanium p-type transistors and achieved state-of-the-art results, even beyond expectations,' confirms Dr Dimoulas.

Results for the n-type transistor were more mixed, but still very positive. The team successfully created an InGaAs transistor and also found a way to arrange them on a silicon substrate so as to keep the fabrication cost low. This was a major result, because there are significant integration and architecture issues when building a III-V-based transistor on a silicon substrate.

Integration for the p-type transistor was much easier, according to the project coordinator: 'Because Germanium and Silicon are both in group IV of the periodic table, their structure is similar and they are chemically compatible so Germanium can be processed in much the same way as Silicon.'

But InGaAs is less compatible with Silicon and has a greater lattice mismatch which leads to fabrication problems. Co-integration of both types of transistors is even more challenging, he adds, but the team developed a new fabrication tool to cope with the issue of growing III-V layers onto a large silicon substrate. Dr Dimoulas suggests further research is needed on the n-type transistor developed in the project.

In addition, Duallogic achieved significant results for a specific kind of transistor architecture called implant-free quantum well transistors, which could lead to microchips that offer even better performance than conventional 'Metal oxide semiconductor' (MOS) transistors.

Industry players

'We were very fortunate to have imec and CEA-LETI in our consortium because, through them, we were able to get access to many industrial players in the semiconductor industry,' notes Dr Dimoulas.

The consortium also hopes to continue the research, ideally in a larger project with more partners, because the results, while state of the art, are not yet at the level where they can be picked up by industry.

'We also want to develop simple circuits, like ring oscillators or inverters, so we are currently looking at appropriate RTD instruments to continue the work,' Dr Dimoulas reveals.

Duallogic's work also has impacts on the advancement of technology options proposed for evaluation by the International Technology Roadmap for Semiconductors (ITRS), which defines the future strategic research axis to achieve further miniaturisation.

'With the help of academics and process developers, the project explored advanced and risky technology options,' notes Dr Dimoulas. This helps industry to identify potentially better solutions for their products, he suggests, saving time and money and allowing them to focus on their shorter-term manufacturing and product development needs.

'The collaboration of "Integrated device manufacturers" (IDM) with equipment vendors in the same project is an excellent opportunity for the nanoelectronics industry to make early decisions about the equipment investments required for future volume manufacturing,' he concludes.

The Duallogic project received research funding under the EU's Seventh Framework Programme, sub-programme 'Next-generation nanoelectronics components and electronics integration'.

- 'Dual-channel CMOS for sub-22 nm high performance logic' project [2]
- Duallogic project data record on CORDIS [4]
- Nanoelectronics Research on CORDIS [5]

- Tiny and tinier: EU projects minimise size of semiconductor chips [6]
- FP6 project to keep EU at forefront of nanoelectronics [7]
- 45-nanometre chips for ultra-fast WiFi [8]
- Copper's not coping: new chips call on light speed [9]

- Country: GREECE
- Information Source: Athanasios Dimoulas, coordinator of the Duallogic project

- Date: 2011-10-26
- Offer ID: 7176

Share this page

Source URL: https://ec.europa.eu/digital-single-market/en/news/microchips-mobile-information-age

Links
[1] https://ec.europa.eu/digital-single-market/sites/digital-agenda/files/newsroom/offer_id_7176_3238.jpg
[2] http://www.ims.demokritos.gr/DUALLOGIC/index.htm
[3] http://cordis.europa.eu/fp7/home_en.html
[4] http://cordis.europa.eu/fetch?CALLER=PROJ_ICT&ACTION=D&DOC=1&CAT=PROJ&QUERY=01323a42f3cc:486b:22a4f053&RCN=85235
[5] http://cordis.europa.eu/fp7/ict/nanoelectronics/home_en.html
[6] http://cordis.europa.eu/fetch?CALLER=EN_NEWS&ACTION=D&DOC=1&CAT=NEWS&QUERY=01323a446242:3c3b:22f852c4&RCN=28948
[7] http://cordis.europa.eu/fetch?CALLER=EN_NEWS&ACTION=D&DOC=2&CAT=NEWS&QUERY=01323a456127:01ae:22f70cbb&RCN=24055
[8] http://cordis.europa.eu/ictresults/index.cfm?section=news&tpl=article&BrowsingType=Features&ID=90773&highlights=microchips
[9] http://cordis.europa.eu/ictresults/index.cfm?section=news&tpl=article&BrowsingType=Features&ID=89457