EUROPEAN COMMISSION

Brussels 8.6.2023
C(2023) 3817 final

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| In the published version of this decision, some information has been omitted, pursuant to articles 30 and 31 of Council Regulation (EU) 2015/1589 of 13 July 2015 laying down detailed rules for the application of Article 108 of the Treaty on the Functioning of the European Union, concerning non-disclosure of information covered by professional secrecy. The omissions are shown thus […] | | PUBLIC VERSION<br><br>This document is made available for information purposes only. |

**Subject:**

**State Aid SA.101202 (2023/N) – Austria**
**State Aid SA.101141 (2023/N) – Czechia**
**State Aid SA.101143 (2023/N) – Finland**
**State Aid SA.101193 (2023/N) – France**
**State Aid SA.101129 (2023/N) – Germany**
**State Aid SA.101210 (2023/N) – Greece**
**State Aid SA.101151 (2023/N) – Ireland**
**State Aid SA.101186 (2023/N) – Italy**
**State Aid SA.101201 (2023/N) – Malta**
**State Aid SA.101171 (2023/N) – The Netherlands**
**State Aid SA.101175 (2023/N) – Poland**
**State Aid SA.101192 (2023/N) – Romania**
**State Aid SA.101200 (2023/N) – Slovakia**
**State Aid SA.101150 (2023/N) – Spain**

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**Important Project of Common European Interest on Microelectronics/Communication Technologies (IPCEI ME/CT)**

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Excellency,

## 1. PROCEDURE

(1) On 7 December 2020, 22 Member States signed a joint Declaration on a European Initiative on Processors and Semiconductor technologies, by which they agreed to work together in order to booster the European Union's (the "Union") microelectronics ([1]) and communication technologies value chain and to strengthen its capabilities to develop the next generation of trusted, low-power processors, thereby attaining the Union's digital targets and digital transformation. In this Declaration, Member States stated their willingness to cooperate and co-invest in semiconductor ([2]) technologies by mobilising industrial stakeholders, aiming towards addressing common challenges through various funding mechanisms and setting up a new Important Project on Common European Interest ("IPCEI").

(2) In this context, multiple Member States launched national calls for preselecting potential projects and, during the period from March 2021 to September 2021, held several technical meetings (with the participation of the European Commission (the "Commission") to design, prepare and develop a common programme for an IPCEI, as well as to receive guidance on how to prepare all the information necessary for the individual project portfolios of the relevant undertakings (the "participating undertakings").

(3) Between 17 December 2021 and 4 March 2022, Austria, Czechia, Finland, France, Germany, Greece, Ireland, Italy, Malta, the Netherlands, Poland, Romania, Slovakia, and Spain pre-notified their plans to participate in an IPCEI on Microelectronics and Communication technologies ("IPCEI ME/CT") on the basis of a common draft overall descriptive text (so called "Chapeau" document) prepared taking into account the criteria of the IPCEI Communication ([3]), as well as detailed information on the proposed IPCEI ME/CT including its components and individual projects.

(4) The Commission requested and received complementary information from all the participating Member States listed in recital (3) (the "Member States") and the participating undertakings during the period between February 2022 and March 2023.

(5) The Commission services organised high-level meetings with senior representatives of the Member States in order to enhance coordination between the Member States

([1]) 'Microelectronics' is the science and technology involved in the design, manufacturing, and use of very small electronic devices and circuits, often referred to as chips or integrated circuits ("ICs"), which are devices that can capture, store, process and act on data. 'Chip' means an electronic device comprising various functional elements on a single piece of semiconductor material, typically taking the form of memory, logic, processor, optoelectronics and analogue devices.

([2]) 'Semiconductors' are the material bases for the chips. It means one of the following: (a) a material either elemental or compound, whose electrical conductivity can be modified, or (b) a component consisting of a series of layers of semiconducting, insulating and conducting materials defined according to a predetermined pattern, and intended to perform a well-defined electronic or photonic functions or both.

([3]) Communication from the Commission, Criteria for the analysis of the compatibility with the internal market of State aid to promote the execution of important projects of common European interest (OJ C528/10, 30.12.2021).

and ensure progress. These high-level meetings took place on 14 October 2022 and on 15 March 2023. In addition, during the pre-notification stage, meetings took place between the Commission and the Member States at the technical level.

(6) On the following dates, the Member States notified under Article 108(3) of the Treaty on the Functioning of the European Union ("TFEU") State aid for the execution of IPCEI ME/CT: Austria, Finland, Ireland, Italy, the Netherlands, Poland, Slovakia on 19 April 2023, Czechia, France, Malta, Spain on 20 April 2023, Greece and Romania on 21 April 2023, Germany on 24 April 2023. All the Member States have individually notified the common Chapeau document and their planned aid measures.

(7) By letters accompanying each notification, each Member State agreed to waive its respective right deriving from Article 342 TFEU in conjunction with Article 3 of Regulation 1 ([4]) and to have this Decision adopted and notified in English.

## 2. OBJECTIVES AND DESCRIPTION OF IPCEI ME/CT

### 2.1. Objectives of IPCEI ME/CT

(8) By participating in IPCEI ME/CT, the Member States have agreed to ensure the further development of the microelectronics and communication technologies value chain by enabling the scaling-up of advanced technologies and the deployment of advanced, 2nd and 3rd generation ("GEN") technologies. IPCEI ME/CT, amongst other things, seeks to contribute to maintaining and boosting the competitiveness of the value chain, as well as ensure that the microelectronics and communication technologies ecosystem remain of strategic importance for the Union also in the future. ([5])

(9) The Member States intend to grant aid to undertakings that will participate in IPCEI ME/CT, in order to develop an innovative and sustainable microelectronics and communication technologies value chain that goes substantially beyond the state-of-the-art. IPCEI ME/CT will bring together undertakings operating at different levels of the value chain.

(10) The overall objectives of IPCEI ME/CT, established in the Chapeau document, are to:

a. reduce the fragmentation of the Union's research, development and innovation ("R&D&I") activities in the area of microelectronics and communication technologies by coordinating technological roadmaps and national strategies;

b. create beyond global state-of-the-art microelectronics and connectivity solutions enabling the digital transformation;

([4]) Council Regulation No 1 determining the languages to be used by the European Economic Community, as amended (OJ 17, 6.10.1958, p. 385).

([5]) https://ec.europa.eu/info/sites/default/files/swd-strategic-dependencies-capacities_en.pdf

c. contribute to the first industrial deployment ("FID") of strategic technologies that offer an alternative to More Moore ([6]) (i.e., More-than-Moore ([7]) and Beyond Moore ([8])), thereby increasing Union's technological presence in the global microelectronics domain;

d. enable the most energy-efficient and resource-saving microelectronics systems ([9]);

e. establish European standards to increase the resilience in data and cybersecurity at all levels of the microelectronics and communication technologies value chain; and

f. contribute to the development of competences and skills, with the aim of attracting private investments and supporting new skilled jobs in the Union.

### 2.2. Description of IPCEI ME/CT

(11) This section describes IPCEI ME/CT as it has been presented by the Member States in their notifications. IPCEI ME/CT is organised along four different work streams ("WS"), as presented in Figure 1, which represent the building blocks that relate to innovations in the area of sensors, high-performance processors, microprocessors including artificial intelligence ("AI"), actuators and communication means for secure data exchange.

([6]) 'More Moore' corresponds to the miniaturisation of the digital functions leading to electronic components benefiting from exponentially increasing computational power from one generation to the next.

([7]) 'More-than-Moore' refers to functional diversification of semiconductor-based devices. It complements digital signal and data processing in a product by combining digital and non-digital functionalities. These functions may imply among others analogue and mixed signal processing, the incorporation of passive components, high-voltage components, microsystems, sensors and actuators. 'More-than-Moore' technologies allow non-digital functionalities, as well as non-electronic information, such as mechanical, thermal, optical, acoustic, biomedical and others, to migrate from the system board-level into the package or onto the semiconductor chip and enable the conversion of non-digital functionalities into digital data and vice versa. Technological progress from one technology generation to the other is not based on pure downscaling of structure widths on the semiconductor chip, but on optimising a variety of parameters on the semiconductor chip as well as of the package design.

([8]) 'Beyond Moore' refers to a concept that overcomes the traditional split between 'More-Moore' and 'More-than-Moore' and proposes to merge elements from both realms.

([9]) 'Microelectonics systems' comprise very small electronic devices and circuits for the collection, processing and transmission of data or signals

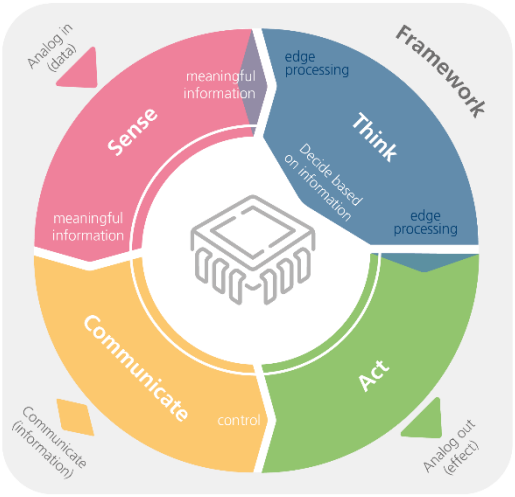


***Figure 1: WS structure of IPCEI ME/CT***

(12) Within each of these WS, the participating undertakings will conduct both R&D&I and FID activities.

*2.2.1. Differences between IPCEI ME/CT and IPCEI in Microelectronics ("IPCEI ME")*

(13) On 13 December 2018 and 23 March 2021 the Commission adopted two decisions not to raise objections on the first IPCEI in Microelectronics ("IPCEI ME") involving 30 undertakings from four Member States and the United Kingdom. ([10])

(14) The scope of the IPCEI ME/CT, as illustrated in the Chapeau document, differs from the scope of IPCEI ME. Although both cover many aspects of the same markets, IPCEI ME/CT has a much broader geographical scope. With the participation of 14 Member States and 56 participating undertakings, IPCEI ME/CT is expected to foster important spillover effects due to the concrete direct participation and significant collaborations between the participating undertakings across the Union. Moreover, IPCEI ME/CT encompasses the involvement of 46 associated participants from multiple Members States, including Belgium, Hungary, Latvia, Portugal and Slovenia, and from Norway (see recital (47) and Annex II).

(15) Furthermore, the IPCEI ME focused on five core areas: energy efficient chips, power semiconductors, smart sensors, digital computing, optical equipment, and compound materials. IPCEI ME/CT instead has a broader focus that includes the entire value chain from materials to system integration. This value chain starts with key raw materials and wafers, novel material integration, along with tools and manufacturing equipment, includes chip design and intellectual property ("IP"), packaging ([11]), assembly, testing, and ends with system integration and validation, including system

([10]) SA.46578 (2018/N) and others - Important Project of Common European Interest (IPCEI) – Microelectronics, OJ C 7, 10.1.2020, p. 1; and, SA.56606 (2020/N) Austria joining the IPCEI Microelectronics 2018 (not yet published).

([11]) Packaging in the semiconductor sector means the process of encapsulating one or more discrete semiconductor devices or IC in a metal, plastic, glass, or ceramic casing during the final stage of semiconductor manufacturing process.

software (“SW”). IPCEI ME/CT will focus on the increasing interconnection between the different levels of the value chain by adopting a coordinated approach.

(16) Moreover, the Member States participating in IPCEI ME/CT note that, although the value chain, and sometimes the type of applications, may be similar, the different individual projects and the planned innovations are different following their own technological paths.

(17) For example, IPCEI ME/CT includes the newest generation of power semiconductors based on silicon carbide (“SiC”) technologies. This generation has significant benefits compared to the previous generations due to the significant development in the materials used in the power semiconductor industry, since the last IPCEI ME. The use of this technology enables greater efficiency of the semiconductors. Therefore, SiC semiconductors can contribute significantly to the Union objective of a green and digital transition as, for example, they allow for a greater range and higher performance of electric vehicles (“EV”), while the size of batteries and the charging time will decrease.

(18) Furthermore, the IPCEI ME developed state-of-the-art technologies for smart sensors. IPCEI ME/CT is expected to go several steps further by addressing not only improved performances for optical (i.e., visible, infra-red (“IR”) in new bands, distance, and combination of several parameters and bands), mechanical (i.e., accelerometers, gyroscopes, and combination of parameters) or magnetic sensors, but also a more extended approach on other sensors, such as radars, light detection and ranging (“LiDAR”) and a combined environment sensing and local low-power embedded signal processing, including the most advanced embedded AI solutions.

(19) In the domain of technologies for digital computing and associated extensions, the IPCEI ME enabled an extended functionality beyond pure digital computing with technology nodes down to 22 nanometers (“nm”). IPCEI ME/CT will advance the complementary metal oxide semiconductor (“CMOS”) technologies by shrinking the dimensions, in order to provide higher performance and lower power consumption. Furthermore, IPCEI ME/CT aims at deploying new generations of fully depleted silicon on insulator (“FD-SOI”), with new embedded computing capabilities, which are expected to enable more efficient internet of things (“IoT”) implementation and edge-AI deployment, avoiding excessive electrical consumption.

(20) Lastly, the IPCEI ME focused on deploying the “Advanced Optical Equipment” technology for the high-numerical aperture extreme ultraviolet (“high-NA EUV”) lithography optics, requiring deployment at 2 nm node. IPCEI ME/CT will aim at developing and deploying disruptive technology solutions, though new designs of optical systems and lithography equipment, as well as manufacturing and metrology equipment and processes, enabling the next technology nodes at 1nm.

#### *2.2.2. Description of the WS in IPCEI ME/CT*

(21) The Member Stated describe that microelectronic systems that are developed to meet the requirements of downstream industries generally consist of four functional dimensions that are essential and highly interdependent.

(22) Important types of semiconductors stand for the organs of perception, such as the eyes, the nose, the skin, the tongue and the ears (WS-SENSE). Without the data gathered by these sensory devices, the combination of processor and memory - being

the brain of a system - (WS-THINK) would have nothing to "think". Work and performance can only be achieved, if the body and muscles (WS-ACT), which communicate with the brain via strong nerve pathways (WS-COMMUNICATE), act together effectively at lowest possible energy consumption and environmental impact. These functional elements are essential for the ongoing digitalisation. Co-design and fine-tuned interaction of these functional elements is essential to generate the intended performance.

#### 2.2.2.1. WS–SENSE

(23) WS–SENSE focuses on the use of sensors to collect relevant analogue signals from our environment and translate them into digital data, with a view to enabling the decision-making of WS–THINK. The applications of sensors are wide-ranging: from observing and predicting the behaviour of road users in order to increase safety, to measuring and predicting the current and future health of patients, to detecting and monitoring greenhouse gas emission levels, and to detecting and sorting materials during recycling.

(24) The overarching objective of WS–SENSE is to enable the development of the next generation of sensor components and systems. The specific needs of the various downstream sectors (such as automotive, industry, healthcare, agri-food, etc.) require that the newly developed sensors be robust, reliable, scalable, AI-enhanced, highly performant and energy- and cost-efficient and that they display novel functionalities.

(25) The participating undertakings will contribute to WS–SENSE with various R&D&I and FID activities. Relevant activities include the development, demonstration and pilot manufacturing of innovative, sustainable and reliable materials; the development of advanced processes, and of characterisation, metrology, inspection and testing equipment, including electronic design automation ("EDA") tools; the development of leading-edge compound materials, perception technologies, micro-electro-mechanical systems ("MEMS") and special sensor components for a large number of applications; the development and prototyping of advanced sensor systems, with a view to improving overall performance and reduce cost; the implementation of advanced manufacturing technologies and processes such as AI-based automation to reduce production cost and environmental footprint; and developing innovative, reliable and cost-effective packaging solutions.

(26) The abovementioned activities are expected to contribute to the following main specific objectives:

- matching the increasingly complex and demanding requirements of downstream sectors, including the incorporation of AI in or close to sensors;
- reducing fabrication costs and broadening the potential applications by integrating different types of sensor technologies into advanced and flexible platforms;
- increasing energy efficiency throughout the sensor's lifecycle, from manufacturing to use, and targeting ultra-low-power consumption;
- promoting the use of sustainable and highly recyclable materials, and ultimately reducing electronic waste; and

- fostering innovation in certain specialized sensing technologies, such as application specific photonic integrated circuits ("ASPIC"), silicon-in-insulators ("SOI"), MEMS, and 3D integration and packaging.

(27) The projects included in WS–SENSE face multiple challenges. In the current process of digital transformation, sectors such as mobility, industry, wearables, telecommunications, aerospace, defence, agri-food and healthcare make increased use of sensing capabilities to optimise monitoring and decision-making. Oftentimes, these sectors have conflicting requirements such as high-energy efficiency and sustainability, and high data handling, high-performance and AI-enablement.

(28) Other challenges include the need to set up a dialogue between all involved stakeholders, including in the framework of standardisation bodies, to calibrate and validate the performance, lifetime and safety of newly developed sensors; and the development of novel packaging and integration concepts as a precondition to integrate several functionalities into a single platform.

2.2.2.2. WS–THINK

(29) WS – THINK aims to develop advanced processing and memory technologies in order to convert the signal inputs (WS–SENSE) into communication signals (WS–COMMUNICATE) and actionable outputs (WS–ACT). Processing and memory technologies are the central decision-making components of information systems, and they must be both secure and energy efficient.

(30) The overarching objective of WS–THINK is to create secure and energy-efficient data processing and memory systems and processes utilising the expertise of the whole microelectronics and communication technologies value chain, including materials, software tools, equipment, front- and back-end technologies, chip design, system integration, and fabrication. The innovative designs, novel materials and equipment will be used to manufacture electronic and photonic technology solutions in a resource-friendly manner for various fields of application.

(31) The participating undertakings will contribute to the WS–THINK with R&D&I and FID activities aiming to develop secure and low-consumption data processing and memory systems and technologies (e.g., advanced wafer substrates, new design and modelling tools, metrology equipment, technology platforms for logic circuits, novel memory chips and technologies, AI chips etc.) These technologies will be developed in close collaboration with the downstream industries where the products and services will be deployed, notably for embedded processing in the automotive, communications, security and health sectors. Efficient embedded processing and edge-AI optimise computing performance in view of power efficiency by reducing the size and latency of data packages that need to be transmitted. This brings systems to a higher level of efficiency and contributes to data protection and privacy at the same time.

(32) The development of the advanced processing and memory technologies in WS–THINK faces multiple challenges. Microelectronic systems need to integrate complex functionalities in an energy-efficient manner. For instance, 5G and 6G equipment needs to integrate multiple functionalities, including radio frequency and analogue communication systems in system-on-chip ("SoC") components, whose size is decreasing constantly. In addition, intelligent power integrated system

solutions and high-performance computing ("HPC") applications need to improve their power-performance balance.

(33) Moreover, the applications need a high focus on energy efficiency in order to bring technology breakthrough for digital frugality whatever the complexity of the system. These requirements need to be balanced with the need for operational performance and security, reflecting privacy demands and the increased threats to cybersecurity.

#### 2.2.2.3. WS–ACT

(34) Following the collection of information from the microelectronics environment (WS–SENSE) and its processing for decision-making (WS–THINK), the aim of this WS is to act on this information, for example by managing the energy flow, displaying or visualising the information, moving or adjusting technical specifications, heating, cooling or driving an electric motor etc.

(35) To this end, the overarching objective of WS–ACT is to enable the design activities and innovative materials for new highly efficient integrated components, modules and smart systems with a high level of performance and for a wide range of applications (e.g., HPC data centres, power storage and conversion for smart grid and renewables, EV, displays, digital health systems, innovative smart manufacturing, robotics etc.).

(36) The participating undertakings will contribute to the WS–ACT with R&D&I and FID activities for the development of several technologies based on semiconductor materials such as silicon ("Si"), SiC and gallium nitride ("GaN"), notably advanced substrates and pressure, volume and temperature ("PVT") equipment, advanced epitaxy, Si-based innovative technologies for smart power, highly integrated technology platforms, power electronics systems and mechatronic systems for power management. All these activities are expected to contribute towards the following main specific objectives:

- meet the needs of the downstream industry;
- improve scalability and modularity and investigate new manufacturing processes for smart and efficient integrations;
- reduce both duration and engineering efforts to design, validate and manufacture power technologies, components and systems;
- increase energy efficiency, thereby contributing to the overall $CO_2$ reduction and to less carbon intensive value chain cycle; and
- promote circular economy and recyclability, resulting to the reduction of the global carbon footprint of the manufacturing value chain.

(37) In order to achieve the WS's overarching and specific objectives, all of the individual projects in this WS face multiple challenges. The constant digitalisation of society inevitably results in a broad scope of applications requiring advanced power technologies and electronic components and systems. Given in addition, the general trend towards electrification in the effort to achieve climate neutrality, especially in the mobility applications, the market has moved towards more complex versions of both digitalised and electrical products, thereby resulting in many industrial sectors

being confronted with the challenge to rapidly address systems with higher and diversified requirements.

(38) Furthermore, a major challenge of the activities pursued in this WS is to balance two conflicting objectives, namely: the objective to increase energy efficiency and achieve climate neutrality with the objective to contribute to the digitalisation of the society, which will inevitably lead to multiplying the uses of electrical energy.

#### 2.2.2.4. WS–COMMUNICATE

(39) Nowadays, the consumers, the enterprises, as well as the public sector, need higher data speed mobile network services with higher performance and reliability. Thus, broadband wireless and wireline secure connectivity is a prerequisite for the digital transformation of processes and services. One of the keys to this digital transformation is the deployment of communication systems with the use of novel and innovative microelectronic components.

(40) The WS–COMMUNICATE addresses microelectronics as related mainly to receiving from and transmitting to electronic equipment information that has been processed in WS–THINK. This transmission requires - among other things - advanced communication infrastructure, edge-computing, devices including IoT and the development of applications for signal and user data processing.

(41) To this end, the participating undertakings will contribute to the WS–COMMUNICATE with R&D&I and FID activities aiming to develop robust, reliable and high-speed communication systems that are expected to improve the current connectivity amongst the various components and users and allow the transmission of greater amounts of information (e.g., advanced materials supporting 5G/6G, photonics technology, advanced piezoelectric materials and processes, advanced packaging technologies , radio and digital signal processing, wireless transceivers for radio systems, edge-cloud and edge-AI solutions etc.). This is expected to enable the development of technical solutions that are in high demand by society such as, virtual calls and meetings, autonomous vehicles, Industry 4.0, smart cities, as well as applications in multiple sectors (e.g., health, agro-food, defence, aerospace, avionics, power plants, etc.).

(42) To meet the above objectives and contribute to the digital transformation, the WS–COMMUNICATE faces multiple challenges. One of the most important challenges is how to master the increasing complexity of the digital transformation that requires high-performance processors and software integration, for example for the virtualisation of hardware (“HW”) and interoperable interfaces of communication systems that are expected to offer more flexibility to new services and industrial processes.

(43) Another key challenge is to manage the huge number of heterogeneous types of communication systems, such as frequency bands, communication topologies, service delivery, as well as access points and mobile terminals that are expected to be significantly different in the hardware settings.

(44) Other challenges include the reduction of the power consumption while maintaining or increasing the performance in terms of speed and bandwidth; the design of new algorithms and architectures needed in communication systems for mobility applications to meet the ambitious emission reduction targets of the Union (see

recital (366)); the need to promote circular economy and recyclability along the microelectronics and communication technologies value chain, aiming at minimising the environmental impact of microelectronics; the development of standardisation in chip and system design, thereby increasing resilience in data and cyber security against increasingly effective attacks; and the security of chip supply by increasing the semiconductor chip design and development technologies for leading-edge communication systems.

*2.2.3. Description of the participating undertakings in IPCEI ME/CT*

(45) This section briefly describes the 56 participating undertakings involved in each WS of IPCEI ME/CT. The individual projects of each participating undertaking ([12]) under the different WS are described in more detail under section 2.4.1.

(46) The participating undertakings, including 15 SMEs, are:

ADVA Optical Networking SE ("ADVA")

ADVA (Germany) is a network equipment manufacturer providing optical network, packet edge and virtualization as well as network synchronization solutions for communication products.

Airbus Defence and Space SAS ("Airbus")

Airbus (France) is an aerospace corporation. It manufacturers aircrafts and various products for aeronautical, space, telecommunication and defence purposes. Furthermore, Airbus provides telecommunication solutions for terrestrial, radio, optical and satellite communications.

Aledia SA ("Aledia")

Aledia (France) is a SME that develops chips for micro-light-emitting-diodes ("mircoLED") used in displays.

Analog Devices International U.C. ("ADI")

ADI (Ireland) designs and manufactures analog, mixed-signal and digital-signal processing integrated circuits ("IC"). The products are used for data conversion, signal processing and power management.

ASML Holding N.V. ("ASML")

ASML (the Netherlands) manufactures photolithography machines and supplies chipmakers with the equipment to produce semiconductors.

AT & S Austria Technologie & Systemtechnik AG ("AT&S")

AT&S (Austria) manufactures printed circuit boards ("PCB") and IC substrates that connect a chip to the circuit board.

([12]) These undertakings will participate in IPCEI ME/CT with separated individual projects implemented by the different legal entities, bringing the total number of individual projects to 68.

AVL List GmbH ("AVL")

AVL (Austria) develops, simulates and tests powertrain systems (hybrid, combustion engine, transmission, electric drive, batteries, fuel cell and control technology) for passenger cars, commercial vehicles and off-road, as well as stationary applications to improve the fuel consumption and drivability and reduce emissions and noise.

Bizzcom, s.r.o. ("Bizzcom")

Bizzcom (Slovakia) is a SME that provides technological solutions for automated machines and devices. The undertaking designs and manufactures devices for industrial applications and provides related support services.

Black Semiconductor GmbH ("BLK")

BLK (Germany) is a SME that develops a graphene-based technology to fabricate integrated electronic-photonic circuits.

Carl Zeiss SMT GmbH ("Zeiss")

Zeiss (Germany) supplies the semiconductor industry with optical projection systems and mask manufacturing equipment for defect inspection, repair, measurement and tuning. The undertaking is a part of the Carl Zeiss Group, a manufacturer of optical systems and optoelectronics.

Codasip s.r.o ("Codasip")

Codasip (Czechia) is a SME that supplies processing solutions for IC designers based on open instruction set architecture to support the development of advanced processors for heterogeneous computing.

Cognitive Innovations Private Company ("Cogninn")

Cogninn (Greece) is a SME that develops technology systems and applications for telecommunication infrastructures. It focuses on 5G and 6G platforms as well as edge-AI systems.

Cologne Chip AG ("Cologne Chip")

Cologne Chip (Germany) is a SME that develops IC for digital telecommunications. The undertaking also licenses building blocks for IC designs and offers a Field Programmable Gate Array ("FPGA") chip.

Continental Automotive France SAS ("Continental-FR") and Continental Automotive Romania SRL, Continental Automotive Systems SRL ("Continental-RO")

Continental (France and Romania) is a supplier of embedded electronics and software for mobility applications. It is part of the Continental Group, which is a supplier for the automotive, transportation and industry sectors and provides brake systems, interior electronics, powertrain and chassis components, tachographs, tires and other equipment.

Continium Technologies s.r.o. ("Continium")

Continium (Slovakia) is a SME that designs IC. The undertaking uses analog-to-digital conversion technology for measurement, sensor and wireless applications.

EEMCO GmbH ("EEMCO")

EEMCO (Austria) designs and builds crystal growth equipment and dedicated furnaces for the SiC single crystal growth process. It is a subsidiary of the EBNER group, which is a manufacturer in the field of high-temperature hot-zone design and plant assembly. It designs and constructs industrial furnaces for the heat treatment of metals.

Elmos Semiconductor SE ("Elmos")

Elmos (Germany) develops and produces semiconductors and sensors primarily for the automotive industry.

Ericsson Antenna Technology Germany GmbH ("Ericsson")

Ericsson (Germany) provides antenna systems for radio access networks ("RAN") and wireless connectivity infrastructure. The undertaking is a subsidiary of the Ericsson group, a network equipment and telecommunication services provider.

Ferroelectric Memory GmbH ("FMC")

FMC (Germany) is a SME that designs ferroelectric memory technology modules for embedded SoC components and standalone memory solutions.

Freiberger Compound Materials GmbH ("FCM")

FCM (Germany) produces semi-insulating and semi-conducting gallium arsenide single crystals and wafers.

GlobalFoundries Dresden Module One LLC & Co, KG ("GF")

GF (Germany) is a semiconductor foundry and manufactures a broad range of customer-specific chips for various applications. The undertaking furthermore offers testing and pre-product services and various packaging technologies.

Infineon Technologies Austria AG ("IFX-AT") and Infineon Technologies AG with Infineon Technologies Dresden GmbH & Co KG, Siltectra Gmbh (together "IFX-DE")

IFX (Austria and Germany) is part of the Infineon group. The undertaking develops and manufactures semiconductor and system solutions for automotive, industrial power control, power and sensor systems, and digital security solutions applications.

Innova IRV Microelectronics S.L. ("IRVI")

IRVI (Spain) is part of the Ricardo Valle Institute of Innovation Foundation. The undertaking develops, integrates, tests, validates, and commercialises microelectronic technologies and products.

Knowledge Development for POF S.L. ("KDPOF")

KDPOF (Spain) is a SME that focuses on high-speed optical communications and develops several semiconductor products.

LYNRED SA ("Lynred")

Lynred (France) designs and manufactures infrared technologies for aerospace, defence and commercial markets. It offers infrared detectors that cover the entire electromagnetic spectrum.

MEMC Electronic Materials SpA ("MEMC")

MEMC (Italy) is a semiconductor manufacturer that is active in the processes of Si ingot growing, converting Si crystals into wafers and epitaxy. The undertaking is a subsidiary of the GlobalWafers group, a manufacturer of Si wafers, SOI and SiC wafers and crystal rods.

Menarini Silicon Biosystems SpA ("Menarini")

Menarini (Italy) is biotechnology undertaking. It provides technology to isolate, study and manipulate rare cells in order to develop personalized medical treatments, for example in oncology. It is subsidiary of the Menarini group, which is a pharmaceutical, biotechnology and diagnostics undertaking.

mi2-factory GmbH ("mi2")

mi2 (Germany) is a SME that offers an ion-implantation process for the manufacturing of semiconductor power devices

Mycroft Mind a.s. ("Mycroft)

Mycroft (Czechia) is active in smart grid data advanced processing.

Nearfield Instruments B.V. ("Nearfield")

Nearfield (the Netherlands) is a SME that develops semiconductor metrology equipment and process control metrology solutions.

Nokia Solutions and Networks Oy ("Nokia-FI") and Nokia Solution and Networks GmbH & Co. KG ("Nokia-DE")

Nokia (Finland and German) provides products and solutions for mobile, fixed, optical and industrial-grade private wireless networks. It is a part of the Nokia group, a telecommunications' network equipment and technology undertaking.

NXP Semiconductors Austria GmbH & CO KG ("NXP-AT"), NXP Semiconductors Germany GmbH ("NXP-DE"), NXP Semiconductors Netherlands BV ("NXP-NL") and NXP Semiconductors Romania S.R.L. ("NXP-RO")

NXP (Austria, Germany, the Netherlands and Romania) is a part of the NXP group, a semiconductor manufacturer of near field communication technology. NXP develops secure contactless identification and communications technologies. It also produces sensors, microprocessors and software for wired and wireless communication.

Openchip & Software Technologies S.L. ("Openchip")

Openchip (Spain) is a SME that provides open source computing solutions for HPC, AI, machine learning ("ML") and deep learning ("DL") applications.

Orange S.A. ("Orange")

Orange (France) is a telecommunication operator offering mobile and fixed broadband connectivity services, as well as information technology ("IT") services for businesses.

ams-OSRAM International GmbH ("Osram")

Osram (Germany) provides optical solutions, from emitters to sensors and software, as well as complete optical systems for the consumer, automotive, healthcare and industrial sectors. Its subsidiary ams-Osram International GmbH supplies a wide range of LED.

Renault S.A. ("Renault")

Renault (France) is a multi-brand automobile manufacturer of a wide range of cars and vans, including electric cars.

Robert Bosch GmbH with Bosch Sensortec GmbH and Robert Bosch Semiconductor Manufacturing Dresden GmbH (together "Bosch-DE") and Robert Bosch SRL ("Bosch-RO")

Bosch (Germany) offers mobility solutions, industrial technology, consumer goods, and energy and building technology. It provides technology, software and services, including IoT cloud services.

Rohde & Schwarz GmbH & Co. KG ("R&S")

R&S (Germany) produces electronic capital goods for industry clients and public authorities. It supplies test and measurement instruments and systems for the evaluation of components for wireless communication and consumer devices. It also provides instruments for setting up and monitoring mobile networks, secure communications and frequency management.

Semidynamics Technology Services S.L.U ("Semidynamics")

Semidynamics (Spain) is a SME that designs microprocessors for AI applications with a focus on the open instruction set architecture called reduced instruction set computer V ("RISC-V").

Semikron Elektronik GmbH & Co. KG ("Semikron-DE") and Semikron Danfoss s.r.o. ("Semikron-SK")

Semikron (Germany and Slovakia) is an integrated device manufacturer of semiconductors for power systems. The undertaking produces Si diodes and thyristors, power modules and integrated systems. It provides assembly and packaging of semiconductors together with auxiliary tasks, including testing and validation.

SGL Carbon SE ("SGL")

SGL (Germany) is an internationally active manufacturer of special graphite and carbon materials, as well as carbon fibre and composite materials. SGL's products are used in a number of different areas, such as the semi-conductor, photovoltaics, and LED industry, the chemical, automotive, and aviation industry, and for energy production and storage.

SIAE MICROELETTRONICA S.p.A. ("SIAE")

SIAE (Italy) provides wireless solutions with focus on point-to-point microwave and radio systems. It offers products and services for backhaul radio and provides microwave systems, multiplexers and network management systems.

Soitec SA ("Soitec")

Soitec (France) designs and manufactures semiconductor substrates for the automotive, IoT, mobile and cloud markets.

ST Microelectronics SA ("STM-FR"), STMicroelectronics srl ("STM-IT") and STMicroelectronics ltd ("STM-MT")

STM (France, Italy and Malta) is part of the STMicroelectronics group, an integrated device manufacturer. It offers customers, access to development and manufacturing facilities to produce a wide range of semiconductors.

Sunlight Group Energy Storage Systems S.A ("Sunlight")

Sunlight (Greece) is present in the energy sector and it specialises in the development and production of batteries and ESS for industrial and advanced applications.

Tachyum s.r.o. ("Tachyum")

Tachyum (Slovakia) is a SME that develops a universal processor for data centres and HPC. The undertaking also conducts research on applications for processor and software development.

Teledyne e2v Semiconductors SAS ("Teledyne")

Teledyne (France) manufactures signal chain semiconductor devices, full spectrum imaging and high-power radio frequency solutions for industrial, defence and aerospace applications.

FEI Electron Optics BV ("Thermo Fisher")

Thermo Fisher (the Netherlands) is part of the Thermo Fisher Scientific group. The undertaking supplies equipment for analysing and measuring sub-micron and atomic structures in the markets of microelectronics, material sciences and life sciences. It offers various microscopy devices and solutions.

TRUMPF Photonic Components GmbH ("Trumpf Photonic")

Trumpf Photonic (Germany) manufactures vertical cavity surface emitting lasers and photodiodes. It is a subsidiary of the Trumpf group, a laser manufacturer.

United Monolithic Semiconductors GmbH ("UMS")

UMS (Germany) is a joint venture owned by Airbus and Thales. The undertaking produces various wafers based on gallium arsenide and gallium nitride technologies for different microwave and mm-wave, as well as high-power applications.

Valeo ("Valeo")

Valeo (France) is an international supplier of a wide range of products to automakers. It develops systems and products that contribute to $CO_2$ emissions' reduction and to the development of intuitive driving and automated vehicles.

Vigo System S.A. ("Vigo")

Vigo (Poland) is a SME that produces photonic instruments based on compound semiconductors. It is an integrated device manufacturer of photonic mid- and far-infrared detectors for rail traffic safety, environmental protection, recycling, industrial, military, safety, science and space applications.

Vitesco Technologies France SAS ("Vitesco")

Vitesco (France) is part of the Vitesco Technologies group, an automotive supplier for drivetrain and powertrain technologies. Vitesco produces electric drives, electronic control units, sensors and actuators, as well as exhaust-gas after-treatment solutions.

Wacker Chemie AG ("Wacker")

Wacker (Germany) produces speciality chemical products using Si and ethylene as raw materials. The undertaking supplies various industries, including semiconductors, automotive and construction, with hyper-pure polysilicon, Si rubbers, wafers and polymer products.

X-FAB France SAS ("X-FAB-FR") and X-FAB MEMS Foundry GmbH with X-FAB MEMS Foundry Itzehoe GmbH (together "X-FAB-DE")

X-FAB (France and Germany) belongs to the X-FAB Silicon Foundries group. It is an analog/mixed-signal and MEMS foundry group. The undertaking manufactures Si wafers for analog-digital IC for automotive, industrial, communication and medical applications.

ZF NewCo IV GmbH with Wolfspeed Germany GmbH (together "ZF")

ZF (Germany) supplies technology systems for the automobile and industry markets. It also provides electrification solutions, including inverter systems for electric powertrain systems.

(47) Furthermore, the IPCEI ME/CT involves multiple associated participants, including 15 SMEs, which although not being part of the notified IPCEI ME/CT, they played an essential role in the shaping of the IPCEI ME/CT, by participating in national selection processes, establishing collaborations with the direct participants,

committing to the generation of spillovers activities and contributing to the initial drafting of the Chapeau document. ([13])

(48) A list of the associate participants of the IPCEI ME/CT is annexed to this decision (Annex II).

### 2.3. Governance of IPCEI ME/CT

(49) A governance structure will be set up for the implementation and monitoring of IPCEI ME/CT. The Member States commit to this governance structure and will contribute to it with alignment of their national strategies and with the development of innovative technologies along the microelectronics and communication technologies value chain. This structure is summarized in the table below:

| | | |
|---|---|---|
| IPCEI Supervisory Board ("SB") | | |
| Transformers Group ("TG") | | |
| Public Authority Board ("PAB") | IPCEI Facilitation Group ("FG") | Commission (guest status) |
| IPCEI General Assembly ("GA") | | |

***Table 1: IPCEI ME/CT governance structure***

(50) IPCEI ME/CT's Supervisory Board ("SB") consists of:

- The PAB, with representatives appointed by the Member States participating in IPCEI ME/CT, each having one vote;
- IPCEI ME/CT's FG, with representatives elected by the GA; and
- Representatives of the Commission, as observers and advisers without voting rights.

(51) The role of the SB will be to supervise, monitor and ensure the implementation of IPCEI ME/CT at large. This concerns, in particular, the monitoring of the progress of the participating undertakings' individual projects, as well as IPCEI ME/CT as a whole. The focus of the implementation of IPCEI ME/CT is both on technological advances, the spillover activities that the participating undertakings have committed to undertake, to disseminate these advances, and the environmental activities that the participating undertakings have committed to undertake, to show compliance with the 'do no significant harm' principle. The SB will also be responsible for the annual reporting to the Commission on the basis of information provided by the FG.

(52) In principle, the SB will meet twice a year. In addition, the SB may meet in extraordinary session to discuss any event relating to IPCEI ME/CT, in particular regarding the potential entry of a new participating undertaking or the exit of an existing participating undertaking. The entry of a new participating undertaking to the IPCEI ME/CT will only be allowed if the application of such entry is approved by the GA within the first six months starting from the notification of the decision

([13]) The associate participants may receive funding under the General Block Exemption Regulation or other national or regional funding schemes, without prejudice to the application of Articles 107 and 108 TFEU.

approving the IPCEI ME/CT to the Member States, and pre-notified to the Commission within two weeks thereafter.

(53) The GA will be organised once a year, gathering all participating undertakings and the representatives of the Member States (and the Commission as observer). At its first meeting, within six months after the Commission's decision approving IPCEI ME/CT, the GA will elect the members of the FG, and it will be responsible for adopting decisions on any changes of the FG's composition. Associated participants and indirect partners (see recital (315)) may participate as observers.

(54) In particular, the GA elects the IPCEI ME/CT's coordinator and the leaders (including their deputies) of each WS, who will be members of the SB. It will also designate a participating undertaking that is a member of the FG, as the key contact for the implementation of the spillover commitments. The GA will take note of any exit decision from IPCEI ME/CT either at the next ordinary GA meeting or by written consultation, teleconferencing or videoconferencing. As from its second meeting onwards, the IPCEI ME/CT conference may take place annually and shall be organised alongside the annual ordinary meeting of the GA.

(55) The FG is composed of a speaker and the deputy, the leaders of the WS (and their deputies) and any additional undertaking's representatives or advisors who have assumed related duties. The members of the FG will change over time to take into consideration the end of participation of the participating undertakings according to their respective individual projects.

(56) It will be in charge of WS coordination, annual reporting, communication, preparation of events, etc. It will drive the overall progress of the WS on a non-confidential basis and establish a permanent interface between private and public stakeholders with the goal of highlighting IPCEI ME/CT's role and impact.

(57) The FG will also be responsible for organising and fostering collaboration and communication within IPCEI ME/CT and vis-à-vis third parties who can potentially benefit from the results of IPCEI ME/CT but who are not participating undertakings. For this, the FG will prepare the annual IPCEI ME/CT conference. The first conference will take place at the latest one year following the Commission's decision approving IPCEI ME/CT. During the conference the participating undertakings will present the main results of their work.

(58) The TG will be appointed by the SB and operate as the executing body of IPCEI ME/CT. It will be composed of up to eight members appointed by the PAB, FG and the Commission. It will issue annual work plans, including work packages, tasks and milestones, to advance and measure the performance of IPCEI ME/CT. Its resources will be determined by the TG and are subject to the approval by the GA.

(59) The TG will be responsible for organising match-making, networking, monitoring and further cooperation activities to intensify the collaboration between partners and with third parties in the wider microelectronics and communication technologies ecosystem. The TG will set up a website to serve as the dissemination and interaction channel of IPCEI ME/CT with entities other than the participating undertakings. The website will host public information about IPCEI ME/CT and the participating undertakings.

(60) For this, the website will list all spillover activities to which the participating undertakings have committed (see section 2.5). This information will be presented in the form of an "Events Calendar" with the concrete dates and a brief description of the activity. The interested community will have the opportunity to register to participate in the activities directly with the participating undertaking who will be in charge of the specific activity. The website will thus also serve as a basis for the annual reporting on the delivery of the committed activities. The TG will collect qualitative and quantitative information on each activity. It may also foresee a restricted area for the participating undertakings to organise the implementation of IPCEI ME/CT.

(61) As regards national governance, the participating undertakings' individual projects are governed by funding agreements to be concluded with the relevant funding authority within each Member State. Such funding agreements impose requirements and obligations towards the administration of any individual project according to the rules set up by the funding authority. The national funding authorities are in possession of the commitments of all participating undertakings. As such, the PAB will be responsible for monitoring the completeness of the listings and announcements of the committed spillover activities and knowledge dissemination.

### 2.4. IPCEI ME/CT as an Integrated Project

(62) The Member States submit that IPCEI ME/CT is an integrated project within the meaning of point 13 of the IPCEI Communication. The Member States explain that IPCEI ME/CT is based on a common programme aiming at the same objectives and is based on a coherent systemic approach, as laid down in the common Chapeau document.

(63) The Member States also explain that the four WS of IPCEI ME/CT as well as the respective individual projects of the participating undertakings are both complementary and significantly add value in order to meet the objective of each WS separately and of IPCEI ME/CT as a whole. The figure below presents the overall structure of IPCEI ME/CT, including the individual projects by the participating undertakings in the four WS:

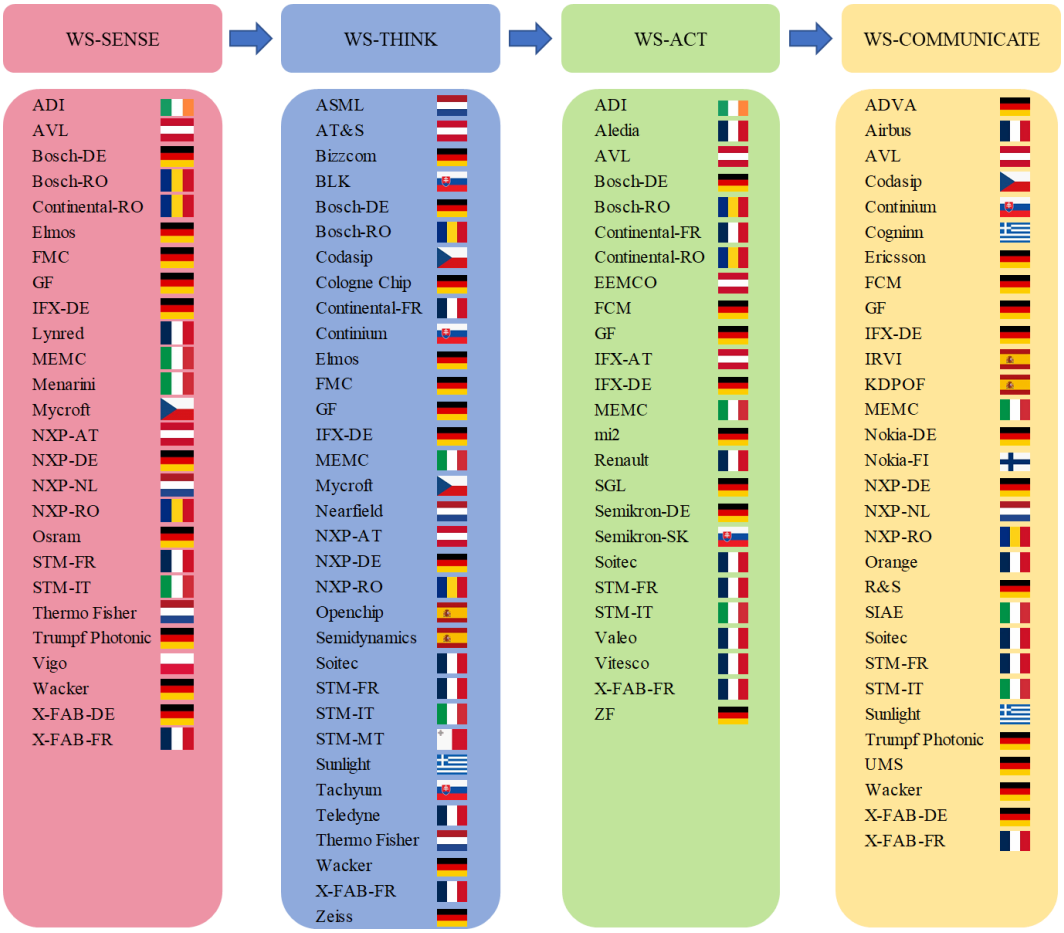


***Figure 2: Overall structure of IPCEI ME/CT***

*2.4.1. Description of the significant added value and complementarity of the individual projects within each WS for the achievement of the objective of IPCEI ME/CT*

(64) The individual projects of the participating undertakings are outlined below in the four WS. Each project is one constituent part of IPCEI ME/CT. In order to facilitate attaining the common objectives, the WS are divided into work packages ("WP"), each one containing specific tasks. The Member States submit that all of the WP with the respective tasks are equally important and complementary and significantly add value for the achievement of the goals of the four WS, as they enable a proper division of the different activities of the participating undertakings and ensure completion of the individual projects in a timely manner.

*2.4.2. Description related to the significant added value and the complementarity of the individual projects for the achievement of the goals of WS-SENSE*

(65) WS-SENSE is divided in four main WP and involves 20 participating undertakings, namely, ADI, AVL, Bosch (Bosch-DE and Bosch-RO), Continental-RO, Elmos, FMC, GF, IFX-DE, Lynred, MEMC, Menarini, Mycroft, NXP (NXP-AT, NXP-DE, NXP-NL and NXP-RO), Osram, STM (STM-FR and STM-IT), Thermo Fisher, Trumpf Photonic, Vigo, Wacker and X-FAB (X-FAB-DE and X-FAB-FR).

(66) According to the Member States, the significant added value of all of the individual projects in WS-SENSE lies in the fulfilment of the common objective to contribute

to digitalisation in order to support the digital transformation of multiple applications, notably mobility, industry, telecommunications, aerospace, medical/health, agriculture/food etc. Furthermore, the WS-SENSE's individual projects will focus on energy efficiency in line with the objectives of the Union Green Deal (see recital (366)), contribute to standardisation activities, thereby increasing resilience in data and cybersecurity, and achieve seamless integration of different types of sensor systems for innovative technologies (beyond conventional Si electronics), aiming towards reinforcing all of the critical parts of the microelectronics and communication technologies value chain.

(67) WP 1 concerns the development of materials, tools and equipment. The respective R&D&I and FID phases contain the following indicative tasks: ([14])

a) exploring and developing eco-friendly materials and substrates for new innovative smart sensors;

b) developing equipment for process, characterisation and metrology inspection, including EDA tools; and

c) designing and implementing methodologies for assembly and testing equipment.

(68) WP 2 concerns the development of semiconductor technologies, smart manufacturing, packaging and testing. This WP contains the following indicative R&D&I and FID tasks:

a) developing advanced thin film technologies for ultra-high performance, to enable the manufacturing of next generation smart sensors;

b) examining new computational, experimental and characterisation tools, their application to the thin film material systems and their integration into sensor devices;

c) developing advanced manufacturing technologies for sensing devices and new production processes for the integration of novel materials into the devices;

d) developing dedicated industrial infrastructure bricks and tools, using Industrial IoT, big data and AI;

e) developing heterogeneous integration technologies and assembly and packaging technologies for microelectronic, optoelectronic and/or microfluidic systems; and

f) conducting advanced testing for integrated sensors.

(69) WP 3 concerns the development of components and modules of sensors used in multiple applications. This WP involves the following indicative R&D&I and FID tasks:

([14]) The Commission has assessed all the notified R&D&I and FID activities and tasks that are included in the various WP of each WS and are part of the participating undertakings' individual project(s). For reasons of brevity and efficiency, the decision provides only some indicative references.

a) developing ultra-low energy sensors for industrial, mobile and IoT applications, sensors for enabling energy efficient systems; and

b) developing sensors for mobility solutions, sensors for environmental protection and food safety, and sensors for a safe and secure digital life and health.

(70) WP 4 concerns the development of sensing (sub-) systems, as well as specific (sub-) system features. This WP involves the following indicative R&D&I and FID tasks:

a) developing technologies for (sub-) system integration and validation of sensors for automotive, environmental protection and energy management applications; and

b) developing technologies for (sub-) system integration and validation of sensors for safe and secure digital life, health, as well as for applications in harsh environments and space.

Description related to the significant added value of the individual projects

ADI

(71) ADI aims at developing a new process platform, combining established CMOS and DMOS processes with novel high voltage devices, advanced passive components and More-than-Moore processing capabilities for a range of new automotive and healthcare applications. In particular, in the automotive sector, ADI is expected to enable the development of multi-turn sensors based on the giant magneto resistive technology, whereas in the healthcare sector, it aims at enabling advances in medical imaging, leading to higher resolution with smaller x-ray doses, and the development of more sensitive core body temperature sensors, thereby facilitating vital signs monitoring.

AVL

(72) AVL's project will focus on the validation, qualification and optimization of ADAS/AD sensors and perception of SW/HW in vehicles. In particular, AVL aims at providing a crucial bridge between chip developers and car manufacturers by increasing beyond the global state-of-the-art the precision of sensor perception and the amount of data that can be processed simultaneously, and by detecting white pots in test scenarios, thereby facilitating driving of vehicles in difficult weather and traffic conditions.

Bosch-DE

(73) Bosch-DE plans to develop a complete portfolio of environmental sensors for highly AD functions and systems, with development spanning from materials to process technology, advanced packaging and system integration. Bosch-DE's project aims at improving the sensors' performance by shrinking the structure sizes and migrating to larger wafer diameters. In particular, Bosch-DE intends to design sensors in advanced nodes, aiming towards realising highly AD and modern vehicle electrical / electronic ("E/E") architectures, including power management IC and microcoulomb ("μC") for steering.

Bosch-RO

(74) Bosch-RO plans to work on the design, prototype and testing of top-of-the-range ASICs, MEMS and integrated sensors and products based on them for the development of robust, reliable, scalable AI-enhanced sensor platforms and components. The added value brought by the project concerns, on one hand, the development of computer vision solutions for the next generation low-power embedded automotive systems and, on the other hand, the deployment of the next generation of ADAS domain controller able to perform perception functions for a wide range of sensors (e.g., video, radar, ultrasound) in different configurations, tailored for the market needs.

Continental-RO

(75) Continental-RO's project plans to focus on the next generation of sensor products for automotive mobility systems. The overall objective is to realise a breakthrough in all of the parts of the value chain for next generation sensor-based systems, meaning from new materials to fully reliable integrated sensor-based systems. In particular, the project will develop and pilot advanced low-power edge-AI, matching low computing power requirements for sensors' micro-controller units ("MCU"). This will aim towards allowing to process sensorial data and to compute predictions, classifications and pattern detection, as well as make self-adaptation on MCU.

Elmos

(76) Elmos plans to develop a novel LIDAR system for distance measurement and gesture recognition. The system will be implemented in solid state (i.e., integrated on a chip without movable parts) and will combine an array of single-photon avalanche diodes with the read-out chips integrated in Si CMOS technology. Elmos' project plans to introduce significant improvements to the existing LIDAR system, feature a better photon detection efficiency and employ AI process for data analysis using the new technology of back-side illumination. It aims at exceeding the global state-of-the-art in terms of pixel number, form factor, and laser driver of the LIDAR system, thereby improving the overall performance of the sensor and employing data pre-processing and data fusion in the controller chip.

FMC

(77) FMC plans to develop a new ferroelectric memory structure suitable for both microprocessor intensive applications and internal non-volatile storage for microcontrollers. That development is expected to yield scalable AI-enhanced miniaturised sensor platforms and components with low-power high-cognition perception systems. Furthermore, FMC's new ferroelectric memory structure aims at monolithically integrating its functionalities in a single flexible platform, which would result in a decrease of fabrication costs, and facilitate virtually multiple applications (e.g., ultra-low energy sensors for enabling energy efficient systems and sensors for automotive mobility solutions).

GF

(78) GF plans to work on customized 5G/6G and novel automotive radar solutions, notably advanced driver assistance systems ("ADAS"). In particular, GF's project aims at focusing on sensor fusion, to bring radar and communication components together in one sensor. Furthermore, it will conduct reliability study of 5G/6G and radar demonstrator based on the development of FD-SOI technology, thereby

enabling faster implementation of the new components and contributing to their digital transformation.

IFX-DE

(79) IFX-DE will contribute to the WS by carrying out R&D&I and FID activities in multiple segments, namely the manufacturing of platforms, the packaging and the development of smart and compound components with high level of integration. […], IFX-DE will develop a beyond the state-of-the-art MEMS platform based […] and system solutions for integrated smart sensors […]. In addition, it will develop new monolithic technology solutions […]. Lastly, IFX-DE will design and develop novel assembly and packaging technologies, including wafer level packaging […].

Lynred

(80) Lynred's project will focus on beyond the-state-of-the-art infrared bolometers and Mercury Cadmium Telluride sensors, notably uncooled micro-bolometer sensors (imagers) for a very wide range of applications in different sectors (including for example consumer electronics, security, health and safety, industry), which are planned to go beyond what currently exists in terms of the noise equivalent temperature difference ("NETD"), pixel pitch, or achieving better NETD values even without the need for image corrections. The project aims furthermore at developing a novel and more reliable cryo-system integrated with a sensor module for earth observations, based on mercury-cadmium-telluride technology, with the aim towards targeting larger sensor areas and less read-out noise.

MEMC

(81) MEMC plans to develop and supply Si wafers with lower power consumption, high level of radiation tolerance and low loss RF communication, aiming at achieving contamination levels (for metal in particular) well below current industry level, as well as specific wafer mechanical characteristics and flatness for materials, such as SOI and GaN.

Menarini

(82) The proposed project aims at leveraging on Menarini's competence in the field of single cell isolation from heterogeneous samples. Menarini plans to combine microelectronics technology (i.e., monolithic CMOS lab-on-a-chip IC and relevant cartridge) with advanced biology, micro-fluidics and AI, thereby delivering a complete, fully automated workflow to isolate, with 100% purity and high throughput, cellular or sub-cellular biomarkers for more automated and comprehensive molecular tests, such as liquid biopsy. This is expected to significantly increase the health-related quality of life for patients including, but not limited, to the relevant case of oncology.

Mycroft

(83) Mycroft's project aims at delivering ultra low-power embedded AI models with on/site ML for ultra low-power IoT devices, with new functionalities having a focus on adaptation, on/site model development directly in the application, higher performance and lower energy consumption due to low requirements on computation capacity and memory. Mycroft's technology is expected to process data inside the

sensor and eliminate the necessity to transfer primary measurements to cloud systems, thereby allowing the development and integration of specialized self-learning AI based sensors in specific technologies and dedicated application domains (e.g., industry, radiation-tolerant sensors and optical sensors).

NXP-AT

(84) NXP-AT aims at developing an advanced ultra-low-power wireless connectivity chipset with ultra-wide band ("UWB") radar sensing and ML capabilities, providing thus, the ability to observe the location of smart devices within a certain area, to limit sensitive use-cases, as well as prevent relaying of confidential information to unauthorised listeners.

NXP-DE

(85) NXP-DE plans to develop radar system solutions for ADAS. This innovation will aim at novel design and production of a specialised More-than-Moore microchip SiP, maximising millimetre wave ("mmW") detection, computing power and integration potential, supporting highly AD requirements (i.e., resolution, classification, segmentation, localisation, mapping), and making these solutions suited for short term market needs.

NXP-NL

(86) NXP-NL plans to develop the overall concepts and design of a leading-edge radar system with a very high-resolution, thereby supporting highly AD requirements (i.e., resolution, classification, segmentation, localisation, mapping), making these solutions suited for short term market needs, and offering the necessary robustness for upcoming interference challenges due to a rising number of radar sensors on the road.

NXP-RO

(87) NXP-RO will aim at developing automotive radar SW tailored to the HW, towards highly AD, whereby enabling an innovation leap in semiconductor technology from 40nm analog to sub-20nm digital radar transceiver. SW R&D will be developed to reach significantly higher angular resolutions using massive-multiple input multiple output ("MIMO") arrays and implementation of ML algorithms, in order to harvest the full potential for the overall radar system.

Osram

(88) Osram work on novel technologies for illumination, visualization and sensing. In particular, Osram's project aims at designing smart and miniaturized compound semiconductor devices for future generations of sensors and emitters, thereby enabling the combination of high-end performance, low energy consumption and multi-functional operation with edge computing and data processing for multiple applications, outperforming the current state-of-art devices, which often require a compromise on performance and energy consumption.

STM-FR

(89) STM-FR will develop a new generation of optical sensors for personal, automotive, industrial, biomedical and IoT domains, aiming at increasing compacity and autonomy. This new generation will enable high level of integration (3D stacking and heterogeneous solutions), innovative pixels merging high resolution and depth sensing, AI in the sensor (deep-edge processing), innovative MEMS, cognitive and multi-spectral sensors able to analyse the ambient or artificial light beyond the visible range.

STM-IT

(90) STM-IT plans to develop a diversified product portfolio of sensor technologies, aiming towards ensuring a smart integration of different components under the same advanced package. This portfolio will include IR MEMS sensors, with a focus on multi-pixel, edge-intelligence engine, bio-inspired MEMS, with a focus on early diagnostic and technology integration of electronics with medicine, and cognitive sensing MEMS with AI capabilities.

Thermo Fischer

(91) Thermo Fisher works on semiconductor equipment manufacturing with the aim to enhance the capability and productivity of transmission electron microscopy ("TEM") workflow solutions, adapted to flexible and high-productive production flow. The significant added value of the project lies in the breakthrough exploration […] to support automation of high-speed end-to-end flexible TEM workflows, thereby enabling semiconductor labs and fabs to take a significant step forward in the optimal use of relevant technologies.

Trumpf Photonic

(92) Trumpf Photonic's project aims at advancing the performance of vertical-cavity surface-emitting lasers ("VCSEL") to enable next generation of optical sensors, through new manufacturing processes, new modelling and material properties. In particular, the project is planned to go beyond global state-of-the-art by improving the power conversion efficiency (>50%) and the device slope efficiency (>2W/A). Balancing losses and the use of stacked junctions connected by tunnel junctions are the basis of new sensor designs.

Vigo

(93) Vigo's project aims at advancing substantially the state-of-the-art in terms of both the planned generic production line and the photonic IC ("PIC") to be produced therefrom. The project foresees the development of PIC-compatible mid-IR light sources and detectors, of the technology of waveguides and passive components, the development of micro-assembly techniques for heterogeneous integration, and of PIC packaging techniques. The significant added value of the proposed project is to define the complete supply chain for PIC operating in the mid-IR part of the spectrum by developing and mastering all necessary technologies and know-how under a single roof, thereby enabling breakthroughs in sensor systems by combining component development, system integration, packaging and cost-effective manufacturing processes.

Wacker

(94) Wacker's project aims at providing a next level polysilicon material for the development of new technologies in the downstream value chain, notably in new, innovative sensing devices. In particular, Wacker plans to develop polysilicon as an essential feedstock for CMOS image sensors, which react extremely sensitive to metallic contaminants by forming pixels in resulting digital images. To this end, Wacker's project will lead to the next levels of purity, low contamination, and high resistivity, focusing on the most detrimental impurities of future sensing devices.

X-FAB-DE

(95) X-FAB-DE will develop technological capabilities for glass wafer processing (mainly in medical and integrated microfluidics devices). To that end, the project will focus on glass wafer patterning, thin film integration and wafer bonding, offering higher chemical stability, compared to Si wafers, as glass as material is well known in terms of biochemistry, e.g., surface functionalization. Furthermore, the use of CMOS wafers instead of passive Si wafers will enable new lab-on-a-chip applications, such as the droplet actuation by the CMOS circuit and/or droplet detection by photo diodes.

X-FAB-FR

(95a) X-FAB-FR will develop innovative designs, architectures and new process flows for the next generation of sensor/driver and communication devices. Main characteristics of these systems include embedded AI, RISC-V photonic capabilities, novel memory concept, energy efficiency and higher operating frequencies.

Description related to the complementarity of the individual projects

(96) According to the Member States, the individual projects in WS-SENSE are complementary because they are covering different elements in the microelectronics and communication technologies value chain. Novel materials and tools within WS-SENSE are expected to lay the foundations for new specialised processing technologies, which constitute the cornerstone for the successful design and production of different types of robust, reliable, and scalable AI-enhanced miniaturised sensor platforms and components with low-power high-cognition perception features to be used in multiple applications, notably automotive, healthcare, IoT, defence etc. Furthermore, the planned innovations on test and measurement equipment and tools are crucial for ensuring the reliability and safety-critical functioning of the developed components and systems.

(97) The complementarity character of the individual projects is illustrated by a number of collaborations within the WS, as explained in section 2.4.7.1.

### *2.4.3. Description related to the significant added value and complementarity of the individual projects for the achievement of the goals of WS-THINK*

(98) WS-THINK is divided into four main WP and involves 28 participating undertakings, namely ASML, AT&S, Bizzcom, BLK, Bosch (Bosch-DE and Bosch-RO), Codasip, Cologne Chip, Continental-FR, Continium, Elmos, FMC, GF, IFX-DE, MEMC, Mycroft, Nearfield, NXP (NXP-AT, NXP-DE, NXP-RO), Openchip, Semidynamics, Soitec, STM (STM-FR, STM-IT and STM-MT) Sunlight, Tachyum, Teledyne, Thermo Fisher, Wacker, X-FAB-FR and Zeiss.

(99) In order to attain the main objective of the WS-THINK to secure data processing and data storage at all levels of the microelectronics and communication technologies value chain in the most energy efficient manner, the participating undertakings are required to bring about significant added value and produce major innovation across various parameters of the WS, notably critical dimensions of chips, usage of new materials, new integration techniques, increased embedded memory density, power efficiency (i.e., the number of operations per second per watt usage), resistance to threat, integration of new standards, denser integration of functions in systems, and virtualisation.

(100) WP 1 concerns the development of advanced materials, including substrates, gases and masks, for new technology generation. It also involves EDA tools and modelling, as well as the development of equipment, assembly, test and inspection systems for new technology generations, 3D integrated SoC and system in package ("SiP"). The respective R&D&I and FID phases contain the following indicative tasks:

a) developing advanced materials including substrates, gases, masks for new technology generations. This task also contains the development of advanced Si wafer substrates and of new material graphene process technology for photonic circuits;

b) introducing new design and modelling tools, to solve issues arising in advanced technologies; and

c) developing new equipment (e.g., litho, deposition, etching and metrology) for new technology generations, including graphene technology. This task also includes the development of metrology and characterisation equipment for new technology nodes.

(101) WP 2 concerns the development of semiconductor technologies and smart manufacturing. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing front-end technology platforms for pure CMOS processes and CMOS with embedded memories, technology platforms based on 2D materials or heterogeneous integration,

b) developing back-end technology platforms for logic circuits and new nanostructures of back-end type; and

c) introducing new methods in manufacturing and supply chain control, such as AI, new automation methods and predictive maintenance.

(102) WP 3 focuses on the development of components and modules. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing general purpose IP and chips for multiple applications, notably, consumers, automotive, HPC, data centres, AI, banking, energy, health, agriculture and IoT;

b) developing AI and HPC IP and chips, automotive and secure IP and chips, and power and battery management IP and chips; and

c) developing novel memory chips and technologies.

(103) WP 4 concerns the development of (sub-) systems for downstream industries, aiming at overcoming current system performance issues and provide functional coverage. The respective R&D&I and FID phases contain the following indicative tasks:

a) designing and developing (sub-)systems for high-performance, cost efficient and energy efficient computing;

b) developing software and virtualisation techniques (including digital twins) and IT infrastructure to support system development; and

c) developing components that comply with environmental conditions and possess cooling capabilities that are required for embedded system and edge-computing and defining specifications for RISC-V based components (e.g., AI/ML accelerators, HPC, sensors and actuators).

Description related to the significant added value of the individual projects

ASML

(104) ASML's project builds on the development of EUV lithography and concerns the development of a high-NA EUV tool. The project is expected to deliver leading edge manufacturing equipment as part of a state-of-the-art sub 2nm R&D pilot line and the creation of beyond state-of-the-art technology solutions to meet future microelectronics manufacturing requirements. The pilot line provides a base for the next generation of advanced nodes solutions, thereby supporting the microelectronics industry accelerate towards achieving leading-edge technology nodes from 2nm onwards.

AT&S

(105) AT&S intends to establish a R&D line and a prototyping and small volume line for advanced IC substrates and advanced packaging technologies (including organic packaging substrates). AT&S plans to research, develop, and subsequently produce the IC substrates for highly advanced nodes (<7nm to sub nm), delivering highly functional, scalable IC substrate solutions for dense packages (6-times higher wiring density), which are expected to enable reduction in power consumption and higher degree of design freedom.

Bizzcom

(106) Bizzcom's project aims at addressing the technological challenge to ensure massive computing capacity for the AI applications through memristor based neuromorphic computation. The project's significant added value is linked to the development of technologies and solutions for AI/ML with high potential in terms of energy efficiency and data security, as well as to the development of chips and embedded systems for specific memristor-based neuromorphic applications. As a result, the project is expected to deploy neuromorphic technologies into commercial products which will represent novel approach for device and equipment manufacturers to implement AI functions (e.g., industrial robots, edge-AI controllers/autonomous devices and industrial connectors).

BLK

(107) BLK plans develop a ground-breaking technology that is expected to enable the fabrication of photonics at the back-end of any electronic circuit, in order to achieve ultrafast chip to chip communication. In particular, BLK's project aims at developing advanced new types of chips based on combining graphene with CMOS technology, thereby exceeding the performance level of these chips, for instance regarding the bandwidth, that is currently possible, and facilitating high volume production.

Bosch-DE

(108) Bosch plans to develop a complete portfolio of vehicle computers for highly AD functions and systems, designed around next generation processors. In particular, Bosch-DE's project aims at improving the processor's performance by advancing the design of high-performance, energy efficient SoC on modern technology nodes and platforms, aiming at developing vehicle computers with larger bandwidth, computing power and storage capacity with significantly reduced component size, power consumption and cost compared to the state-of-the-art.

Bosch-RO

(109) Bosch-RO plans to develop a new centralised and customisable AI-enhanced SW platform for highly AD based on multi-modal sensor fusion and integrated in a centralised E/E architecture. The significant added value concerns the newly developed ADAS system domain controller with computer vision solutions, which will be based on a centralized structure employing a unique ECU, as opposed to multiple ECUs in the current global state-of-the-art, thereby leading to a lower vehicle response time (i.e., duration between sensing and acting).

Codasip

(110) Codasip's project aims at addressing the increased computational requirements of emerging applications (e.g., AI, virtual reality ("VR"), augmented reality ("AR") and 5G/6G communications) and existing applications (e.g., embedded, server, wireless and networks) through the development of new EDA tools for processor design and the development of new high-performance RISC-V processor cores. Codasip will develop specialised architectures that are optimised for specific computational workloads, thereby allowing to increase performance and minimise processors' power consumption.

Cologne Chip

(111) Cologne Chip aims at developing a next generation FPGA, combined with a quasi-analog AI circuit to meet the requirements of modern programmable logic for a wide range of applications, particularly for next generation technologies in the field of AI. The FPGA will be developed in the 5-7 nm process node to enable high-performance and energy-efficient circuits on the chip surface. Furthermore, the FPGA's architecture will be optimised for a greater logic density and shorter signal propagation times, compared to the state-of-the-art, and will display efficient interfaces for high-volume data exchange.

Continental -FR

(112) Continental-FR plans to work on a new large-scale electric/electronic architecture for vehicles through the development of HPC and zonal control units ("ZCU"). The project aims at enhancing embedded SW and HW to allow for numerous digital updates and upgrades over time that are expected to increase the life duration of the vehicle beyond the global state-of-the-art. Moreover, the project will entail the HW implementation of AI through a higher-node technology with low-power consumption and minimal footprint, while sustainability will be enhanced with respect to materials, energy, water consumption and greenhouse gas "GHG" reduced emissions.

Elmos

(113) Elmos aims to develop a chip architecture for sensors and actuators, which includes a hypervisor for increased safety and security, and a microcontroller. The technical challenge is to implement the improvements within the limited computing and memory resources to comply with power consumption constraints. To this end, Elmos plans to build the chip architecture on a Si CMOS platform, combining two dies in one package, with the use of advanced packaging and assembly technologies and the development of new test concepts, using novel SW and AI/ML processes in sensors and actuators outside the central control units, as hypervisors have so far only been realised in the central computing units of automotive systems.

FMC

(114) FMC plans to develop a new ferroelectric memory structure suitable for both microprocessor intensive applications and internal non-volatile storage for microcontrollers. The cell structure does not differ from the traditionally experimented ones, but the choice of new materials (e.g., HfO2) is expected to allow for a drastic reduction of the occupied area on chip and improve the memory cell, material, design and architecture, thereby achieving high cycling stability and speed, data retention properties and novel chip concepts suitable for AI.

GF

(115) GF plans to develop fabrication technologies for high-performance, secure and energy-efficient semiconductor chips. This includes new add-on functionalities and design environments for the technologies from 55nm down to 22nm, new embedded non-volatile memory ("NVM") functionalities, as well as the development of the next generation of 22nm FD-SOI technology. GF plans to develop these technologies with the use of heterogeneous integration and smart manufacturing (e.g., AI methods), thereby combining active optical functions together with energy efficient logic operations in one package, aiming for significant improvements in power consumption and computational performance.

Continium

(116) Continium' project aims at developing different data converter ASICs for sensor readout electronics, including analog circuit design for 12-16 Bit A/D converters and up to 20 Bit D/A converters. In particular, the project focuses on ADC for sensor readout and DAC for sensor stimulation integrated on the smallest chip area of direct partners chip products. For both products, the key innovation concerns the design of the data converters with advanced functionality (bit accuracy reconfiguration, joint

reconfigurable A/D and D/A converter functionality using shared analog circuit blocks) and ultra-low-power (µW) operation.

IFX-DE

(117) IFX-DE's project aims at developing intelligent integrated systems and concepts for power and sensor solutions, including through new AI approaches, […]. The development activities cover […], and address the integration of digital components with power and sensor solution in order to improve energy and process efficiency, increase manufacturing flexibility of different components and reduce system cost dependence on individual applications.

MEMC

(118) MEMC's project aims at developing Si wafers with very tight customer tailored controlled thickness and resistivity combined with extremely low defectivity and energy consumption, resulting to faster signal processing of logic and processing units. MEMC will use EUV lithography tools, in order to access the lowest achievable nodes, to allow the tight control of wafer surface flatness (including the very edge of the wafer), as well as wafer shape and surface defectivity.

Mycroft

(119) Mycroft's project aims at developing autonomous, high frequency, low-power AI for microcontrollers for new generation of adaptive IoT devices. Such a solution represents a key gap-filling technology for the whole IoT devices value chain and for a new generation of sensors. In comparison with the existing IoT sensing devices with a lifecycle limited by the battery life to 6-8 years, battery-less self-learning adaptive IoT devices will allow much cheaper management of large IoT networks, less communication bandwidth and costs, higher predictability and effective data acquisition.

Nearfield

(120) Nearfield plans to develop a fully automated in-line inspection and metrology system that enables non-destructive parallel scanning of an ultra large area of at least a complete chip, catering for advanced-node semiconductor manufacturing processes. Nearfield's new system is expected to offer next generations of advanced-node semiconductor manufacturing processes extreme reliability and reproducibility in high-speed process development […] and control solutions.

NXP-AT

(121) NXP-AT envisages to develop an optimised chipset with a RISC-V based system, resilient against post-quantum cybersecurity attacks, and designed for multiple functionalities in mobile applications. Furthermore, it will focus on a synchronised high-speed battery communication, including the development of innovative IP blocks for battery management systems ("BMS"), thereby enabling safe, smart and secure communication and control systems for best possible energy efficiency in EV, extended range and higher user satisfaction.

NXP-DE

(122) NXP-DE aims at developing next generation of high-performance microcontrollers and microprocessors based on processors in ≤5nm technology nodes with a focus on IP design, microarchitecture and integration of AI. This innovation will enable a powerful microprocessor with ultra-low-power consumption, which aims at combining compute and data power at highest level of cybersecurity and functional safety.

NXP-RO

(123) NXP-RO will introduce next generation SW solutions enabling automotive AD. It plans to improve the current SW solutions and move to ≤5nm technology that serves the future domain and zonal car architectures. These solutions include new infrastructure middleware and drivers for high-speed communication interfaces, power management, ML accelerators and compiler and debugger technologies for new core and accelerator architectures based on the emerging RISC-V open-source cores.

Openchip

(124) Openchip's project aims at developing HW and SW for computer accelerator cards supporting 64bit high precision data, using the latest CMOS technology node and targeting applications in HPC, AI and ML. The main key performance indicators targeted include a computing speed of 160 trillion floating-point operations per second with an efficiency of 115 billion floating-point operations per second/watt using a 256 gigabyte per second memory. Furthermore, the CMOS technology nodes to be used are expected to go from 16-10 nm currently to 2-3 nm for generation 4 (depending on technology available by the external chip manufacturers). Thus, Openchip targets the improvement in performance, energy efficiency and ease of use for high precision accelerators.

Semidynamics

(125) Semidynamic's project aims at developing a new SoC-based AI processor […], using […] technology for memory. The project is expected to deliver a higher speed than the current tensor processing engines […] and provide a significantly better memory subsystem.

Soitec

(126) Soitec's project aims at developing a new generation of FD-SOI substrate meeting the requirement of AI technologies. This new substrate will increase the energy efficiency of AI applications, reduce the size of analog blocks, while ensuring optimal RF connectivity. Furthermore, Soitec will develop a new generation of 2.5D/3D layer transfer technologies for HPC and highly integrated electronic systems. Innovations in layer transfer will make it possible to create 3-dimensional systems with extremely fine granularity (10 to 100 times greater than the state-of-the-art), as well as easy to implement, more effective and cost-efficient packaging solutions that are available for both high-performance and embedded systems.

STM-FR

(127) STM-FR will contribute to this WS by developing new technologies of digital core dedicated to applications requesting fast and low-power embedded processing capabilities, thereby enabling greener and more secure processing. This next generation will include an advanced FD-SOI 18 nm node, dedicated embedded AI architecture, advanced microcontrollers and microprocessors, secure digital and memory technologies, as well as reinforced packaging solutions.

STM-IT

(128) STM-IT's contribution in this WS lies in the development of a variety of new technologies, which are expected to embed new AI methodologies for implementation in IoT nodes, and improved information security methods for verifying secure embedded processing on peripheral microcontrollers. In particular, STM-IT plans to develop […] microcontrollers, as well as create new digital memory nodes based on phase-changed materials ("PCMs"), and advanced microcontrollers and microprocessors with innovative NVM.

STM-MT

(129) The goal of the project is to create the most advanced and highest quality-grade packaging technology for high-end microcontrollers, targeting ADAS automotive application. This technology is expected to optimise the trade-off between flexibility, volume productivity and cost efficiency for advanced packaging and testing, going beyond the state-of-the-art on fab automation and AI/ML on production systems, targeting the most advanced methodology of smart factory and Industry 4.0.

Sunlight

(130) Sunlight will improve and optimise the battery performance to be used in the production of renewable energy. Sunlight will design and develop new IC, application-specific integrated circuits ("ASIC") and MCU for BMS, which introduce the capability to predict the state-of-health of a battery, based on AI functionalities and improved IC packaging and PCB assembly. As a result, the new battery is expected to recognise a potential malfunction before it occurs, hence enabling the balancing of energy consumption in the battery cells.

Tachyum

(131) Tachyum's project aims at developing a high-performance universal processor unifying the functionality of central processing unit ("CPU"), graphic processing unit ("GPU") and tensor processing unit ("TPU") into a single device resulting in energy efficiencies and high performance for high-end computing. The processor is expected to be based on a simple SW model able to dynamically switch workloads and applications, along with easy deployment and maintenance. Tachyum's universal processor will use location-aware processing architecture that improves the efficiency of processor technology by largely eliminating "data bypass" (the act of sending the data required for an operation, to the location where that operation is loaded and ready to be performed) that consumes significant amount of power and impacts the speed of today's processors.

Teledyne

(132) Teledyne's project aims at developing low volumes advanced SiP products and related chiplets and medium volumes flip-chip advanced packaging capabilities, as well as SiP services stemming therefrom. Teledyne's significant added value lies in the fact that its activities are expected to cover successive SiP product generations and chiplets (e.g., SiP with data converters and visual sensors), while enhancing their performances beyond the global state-of-the-art, and to scale-up its advanced packaging flip-chip capabilities from low to medium volumes for possible space applications.

Thermo Fisher

(133) Thermo Fisher plans to work on semiconductor equipment manufacturing to enhance the capability and productivity of TEM workflow solutions and strengthen the digital capabilities along the semiconductor equipment value chain, […]. The project aims at exploring […] TEM techniques to yield near atomic resolution 3D information on semiconductor samples, overcoming the global state-of-the-art […]. It will furthermore develop a comprehensive set of model-based systems engineering and digital twinning (techniques to increase the speed of innovation from concept to market-ready solutions […].

Wacker

(134) Wacker's project aims at providing a next level polysilicon material for the development of new technologies in the downstream value chain, notably in new, leading edge-nodes and devices. In particular, Wacker plans to develop polysilicon as an essential feedstock for leading edge-nodes (e.g., 2nm), which will be composed of billions of transistors on a single chip. Wacker's project will lead to the next levels of purity, low contamination, and high resistivity, by removing the metallic contaminants, which have the potential to deteriorate transistor performance and lead to a complete failure, thereby negatively impacting the chip performance.

X-FAB-FR

(135) X-FAB-FR will develop power efficient in-memory-computing, where a 2-times faster embedded NVM will enable more demanding smart applications, such as smart sensor and smart drivers in EV. X-FAB-FR will also develop edge-AI technologies, requiring AI based embedded computing elements for smart SOC. As a result, data transfer would not be necessary anymore between the computing unit and the data stored in memory, thus saving time and energy. Moreover, volatile additional memory would not be any longer required for AI computation, thereby dramatically reducing footprint and energy. In addition, the company will aim at lowering energy consumption and overall system energy consumption by developing IC technology for smart battery management systems ("BMS").

Zeiss

(136) Zeiss' project addresses R&D on EUV lithography optics and photomask equipment with increased performance as well as repair, measuring, and inspection tools. Zeiss aims at surpassing the current state-of-the-art optics in terms of optical resolution, product overlay, aberrations, and thermal resistance. Supplying these most advanced optical projection systems to semiconductor equipment manufacturers is expected to enable the production of equipment that would allow faster manufacturing of more

advanced chips with smaller feature sizes, thereby making such chips more performant in terms of processing speed and power as well as lower in energy use.

Description related to the complementarity of the individual projects

(137) The Member States submit that the individual projects in WS-THINK are complementary because they are distributed along the microelectronics and communication technologies value chain, allowing advances in materials, tools and substrates enable innovative technology platforms, which are planned to be developed during IPCEI ME/CT. In turn, these technology platforms aim at resulting in more functionally powerful chip designs, which are expected to benefit the multiple applications developed by the individual projects during IPCEI ME/CT.

(138) The complementarity character of the individual projects is illustrated by a number of collaborations within the WS, as explained in section 2.4.7.1.

### *2.4.4. Description related to the significant added value and complementarity of the individual projects for the achievement of the goals of WS-ACT*

(139) WS-ACT is divided into four main WP and involves 20 participating undertakings, namely ADI, Aledia, AVL, Bosch (Bosch-DE and Bosch-RO), Continental (Continental-FR and Continental-RO), EEMCO, FCM, GF, IFX (IFX-AT and IFX-DE), MEMC, mi2, Renault, SGL, Semikron (Semikron-DE and Semikron-SK), Soitec, STM (STM-FR and STM-IT), Valeo, Vitesco, X-FAB-FR, and ZF.

(140) The individual projects of the participating undertakings will contribute to this WS by providing significant added value to meet the challenges of the green and digital transition, by creating more efficient solutions with higher level of performance (e.g., Si based or wide bandgap ("WBG") technologies), for multiple emerging markets and applications. These applications (e.g., energy generation and storage, mobility, data centers etc.) require more efficient power electronics, with higher blocking voltages, lower power dissipation and higher switching frequency.

(141) WP 1 concerns the development of new innovative technologies for simulation tools, equipment, materials and substrates. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing modelling and simulation software to support development and characterisation of both Si and wide bandgap semiconductor devices;

b) launching the next generation assembly and test equipment, as well as a new energy filter-based ion-implantation system concept to meet the challenges posed by these new materials, while guaranteeing the lowest total cost of ownership;

c) developing novel coated graphite components for semiconductor processing, such as epitaxy, metal organic chemical vapor deposition ("MOCVD"), and physical vapor transport ("PVT"), aiming towards longer lifetimes and higher product quality;

d) developing advanced materials and processes for supporting beyond state-of-the-art Si power as well as wide bandgap technologies, especially SiC, GaN

and advanced gallium arsenide ("GaAs") with different wafer substrate diameters (100 mm, 150 mm, 200 mm and 300 mm); and

e) developing new infrastructures and tools, using IoT and AI/ML, thereby ensuring higher productivity, and quality, automatic scheduling, advanced process control on manufacturing equipment and facilities, and cost efficiency.

(142) WP 2 concerns the development of semiconductor technologies, smart manufacturing, packaging and testing. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing advanced Si based power technologies in 200 and 300mm, offering several opportunities for reducing the overall emission level, thanks to significant improvements in function integration, digital computational capacity and performance;

b) developing WGB technologies (including materials, processes and component's architectures), in particular SiC and GaN and GaAs, which are expected to enable components to increase power efficiency and work at higher frequency;

c) developing actuation and harvesting manufacturing technologies and processes, especially for MEMS devices; and

d) developing new infrastructures and tools, using IoT and AI/ML, thereby ensuring higher productivity, and quality, automatic scheduling, advanced process control on manufacturing equipment and facilities, combined with innovative solutions for data analysis systems.

(143) WP 3 concerns the development of components and modules, smart manufacturing, packaging and testing. The respective R&D&I and FID phases contain the following indicative tasks:

a) designing new trustworthy components to enable the future product roadmaps in downstream markets, enabling energy efficiency, transport, electrification, and digitalisation;

b) designing power SiC and GaN components to ensure energy efficiency, and enable the long-term transformation of automotive, production machinery, renewables and other important technology sectors;

c) designing power packaging and modules' components (i.e., package prototypes, including panel level packaging ("PLP") and heterogeneous integration technology and reliability testing for product qualification); and

d) designing actuators and microLED that visualize data and new components and modules for power efficient displays and projector technologies; and

e) developing heterogeneous energy harvesting and storage for autonomous node applications enabling IoT and smart manufacturing.

(144) WP 4 concerns the development of (sub-) systems, smart manufacturing, packaging and testing. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing new electronic PCB, which are expected to implement new components/modules combined with state-of-the-art technology;

b) performing a smart system integration of the electronic components such as PCB, and all the associated functionalities related to the electronic system such as transformers or interconnections between PCB and components, with the aim of significantly improving efficiency and power density while achieving best compromise with packaging ability, cooling, reliability, and durability; and

c) integrating and validating mechatronic power electronics (sub-) systems using Si- and/or wide bandgap MOSFET, as well as novel technologies, such as for example, thermal conditioning of electronic components, that can be easily integrated into downstream application products (e.g., electric powertrain) or testing equipment (e.g., control benches).

Description related to the significant added value of the individual projects

ADI

(145) ADI will contribute to this WS by developing Si smart power and wide bandgap power electronics, with the aim to support the increasing range of operating voltages that can be monolithically integrated on a single wafer, thereby allowing the development of components for the automotive, industrial and healthcare sectors.

Aledia

(146) Aledia will work on 3D microLED chips used in displays, based on a unique architecture using GaN on Si nanowires. In particular, Aledia's project aims at implementing a pilot line for smart pixel processing, and enabling hybrid bonding techniques, which are currently implemented on 200mm Si wafers, to evolve towards 300mm Si wafers for high-volume production. The project will go beyond the global state-of-art by substituting space and energy consuming liquid crystal display ("LCD")/thin film transistor ("TFT") technology displays with much more efficient, more flexible and better performing smart pixel technology displays.

AVL

(147) AVL's project will focus on the validation, qualification and optimization of power electronics (e.g., GaN, SiC) in vehicles. In particular, AVL aims at providing a crucial bridge between chip developers and car manufacturers by increasing beyond the global state-of-the-art the efficiency of the inventers in the vehicle, by supporting 1200V inverters and by achieving higher switching frequencies for the efficient operation of inventers, in interaction with the battery and the e-motor.

Bosch-DE

(148) Bosch-DE plans to develop next generation Si mixed-signal and power processes on 200mm and 300mm wafer-size. Special emphasis is expected to be given on the development of technologies for SiC and of a novel approach on GaN, aiming at significantly increasing the equipment's and the technology's performance, for example, by developing new functional designs, shrinking the structure's sizes, migrating to larger wafer diameters and developing new device concept/topologies.

On the module level, Bosch-DE intends to develop Si-based micro-electro-mechanical actuators for photonic applications, e.g., MEMS-based actuators for photonic display applications in AR glasses, thereby revolutionising the way users interact with data and cloud solutions.

Bosch-RO

(149) Bosch-RO's projects aims at developing integrated smart actuators for EV. The project is expected to overcome the global state-of-the-art by addressing the design, simulation, characterisation, testing and qualification of a novel integrated smart actuator matching with new electrical/electronic (E/E) architectures for high energy efficiency EV, including novel smart actuator employed in oil cooling system, able to withstand harsh environment operating conditions.

Continental-FR

(150) Continental-FR plans to work on a new large-scale electric/electronic architecture for vehicles through the development of HPC and ZCU. The project aims at introducing new generation components (e.g., eFuse, ethernet field bus, safe state components etc.), thereby aiming at improving the level of integration and allowing for the modularity, scalability and upgradability of the electric/electronic architecture. This will make it possible to overcome current state-of-art architectures, which are not capable of accepting evolutions, updates and upgrades over the vehicle lifetime due to their specialized, optimized and limited components.

Continental-RO

(151) Continental-RO's project plans to focus on novel solutions for automotive mobility systems. In particular, the project aims at enabling a smooth transformation of the design and manufacturing processes of the automotive sector, which is still at an early stage, by contributing to the European goal of digitalization though the development of new components and modules for power efficient displays and projector technologies. To this end, Continental-RO will tackle major technological issues along the entire value chain of micro-LED semiconductor technology, by introducing the use of such components and modules in the automotive sector.

EEMCO

(152) EEMCO's project concerns the development of furnaces dedicated to SiC single crystal growth process, for the production of 6" and 8" – SiC single crystal boules and ingots. The project is expected to enable a capacity increase for wafers, with almost twice the useful area for manufacturing IC compared to 6" wafers, delivering 1.8 to 1.9 times as many working chips. Moreover, it plans to fulfill the requirements of thin wafering technologies and reduce wafer thickness by at least a factor 3 to current standard of 350µm, thereby significantly contribute to circumvent the shortage of wafer material.

FCM

(153) FCM's project aims at the development of high performance III-V-semiconductor substrates focusing on the upscaling of GaAs substrate wafer from 6" (state-of-the-art) to 8" for µLED application and GaN substrate wafer from 2" (state-of-the-art) to 4" for highly efficient power electronics. Specific work objectives of the project

concern the development and adaptation of the manufacturing technology (crystal growth, wafering), including the establishment of a pilot line, for larger substrate diameters and the achievement of a wafer quality suitable for the targeted applications.

GF

(154) GF's project will entail the development of CMOS technology functions for display driver interface chips, the development of power technology components for actuators and power-management systems, as well as the development of technology for energy harvesting solutions in CMOS chips. With these work packages, GF aims at developing semiconductor technologies for energy-efficient, sustainable and secure microelectronics for multiple applications (e.g., automotive, industrial, 5G/6G communication systems and defence).

IFX-AT

(155) IFX-AT's project will contribute to the development of next generation of WBG based power electronics at 200mm, including the base material and the subsequent manufacturing process up to the system solution level, aiming at performance improvement in terms of energy efficiency or base material efficiency spanning from 25% to 45% compared to the state-of- art. The project will also contribute to the development of Si based 300mm power electronics, through a new device concept enabled by the development of ultra-thin wafer production technologies and a comprehensive model-based virtual technology development on key processing steps, aiming at significant performance improvements in terms of power efficiency, in the order of 25% compared to the state-of-the-art.

IFX-DE

(156) IFX-DE will contribute to this WS by developing innovative materials and substrates, and smart manufacturing concepts in production systems for SiC power devices and Si based power technologies for front-end platforms. In particular, IFX-DE's project will focus on the development of […] with improved current / power density, as well as […] to enable significantly lower power consumption […] for high-efficiency power transistors in the e-mobility, renewables and industrial applications. […] It will also contribute to developing new generations of SiC based power electronics systems with activities including wafer material, back-end, and system integration.

MEMC

(157) MEMC's project aims to design extremely low resistivity substrates […] on both 200 and 300mm diameters, utilizing special dopants […], which will be used for the development of Si wafers with reduced power consumption, improved drain-source on resistance, higher frequency response and thermal resistivity.

mi2

(158) The aim of the project is to strengthen and advance mi2's doping technology of SiC wafer substrates up to first industrial use and enable the production of high-grade semiconductor components at low cost. In particular, mi2 will implement an industrial-grade ion-implantation system, called EFIITRON ion implanter, and

deliver relevant energy-filters components, with the aim to facilitate market penetration of SiC power devices and improve the reduction of the global carbon footprint of the SiC chip manufacturing value chain.

Renault

(159) Renault will work on the development of WBG devices, actuators and system-level integration technologies. The project's significant added value concerns the implementation of new generation of SiC & GaN transistors in automotive power electronics systems for better efficiency and higher voltage scalability, as well as the development of smart modular architecture and advanced packaging for efficient automotive power electronics systems. Such solutions will allow to reach advanced and efficient power electronics, with higher blocking voltages, lower power dissipation, and higher switching frequency, thereby enabling applications for downstream industries.

SGL

(160) SGL will work on semiconductor production equipment and develop […] carbide-[…] coated graphite components for semiconductor processes, mainly wafer carriers and crucible setups for crystal growth. The improved quality of these components is expected to reduce the total cost-of-ownership for end users and improve the quality of the obtained semiconductor products.

Semikron-DE

(161) Semikron-DE will develop new power semiconductor Si diodes and power modules targeting the system integration requirements for automotive type applications in passenger and commercial vehicles with water cooling. The Si diodes and power modules developed will feature significantly improved power density, efficiency and reliability.

Semikron-SK

(162) The project's objective is to increase the performance of advance manufacturing techniques for semiconductor-based power module packages for renewable energy and industrial applications. Semikron aims at developing an advanced manufacturing facility based on all-in-one technology and digitalisation with potential scale-up of production capacity for innovative power modules. The main contribution will focus on optimised packaging leading to higher efficiency at system level but also on increasing the power density and overall higher performance, with improved reliability, lifetime and robustness.

Soitec

(163) Soitec will deploy its proprietary Smart Cut™ SiC technology to transfer a thin film of an expensive, high-quality SiC wafer into a low-cost, high-conductivity support, increasing the number of components made from the initial SiC wafer. This project includes the deployment of smart SiC substrates in 150 and 200 mm diameters and aims at contributing to securing a European supply chain for SiC material, which is particularly strained because of the increase in volume of EV.

STM-FR

(164) STM-FR will develop new technologies and components for power applications, aiming at contributing to greatly reduced energy consumption. These new technologies will require the development of a first generation of power GaN components, as well as first worldwide 200 mm pilot line, a dedicated packaging of technologies and processes for Si or power GaN devices and related modules, innovative technology options and designs for power Si components.

STM-IT

(165) STM-IT's contribution to this WS lies in the development of new smart power bipolar-CMOS-DMOS ("BCD") products that aim at enhancing power management and motor control devices. It will also aim at introducing high-voltage power components based on the new monolithic GaN technology and WBG MOSFET, as well as new micro-opto-electro-mechanical systems ("MOEMS") and ultrasound devices for data collection. Finally, STM-IT plans to develop energy efficiency and harvesting solutions for applications based on the use of remote and autonomous sensing and actuation devices.

Valeo

(166) Valeo's project aims at developing solutions to maximise the total energy consumption reduction of automotive components and vehicles, by developing a new generation of "energy-intelligent" electronic products. The project entails the use of WBG semiconductors (i.e., SiC and GaN) rather than Si, […].

Vitesco

(167) Vitesco will develop a high voltage box ("HV Box") for EV combining a high voltage bi-directional analog converter ("AC") on-board charger with a low voltage DC-DC converter from high voltage power net, based on new WBG chipset technologies. These technologies will enable a size reduction of the chipset components and a power density increase, with the purpose of enabling the introduction of the new components' placement manufacturing technologies, as well as new possibilities for interconnections.

X-FAB-FR

(168) X-FAB-FR will develop smart chips and drivers, aiming towards improving energy efficiency in applications where electric energy is used. In particular, advanced on-chip drivers with lower on-resistance will enable light emitting diodes ("LED") and brush-less direct current ("BLDC") motor drives with higher energy efficiency solutions than current state-of-the-art for demanding operating conditions, such as the automotive market.

ZF

(169) ZF's project will focus on the development of next generation of SiC chips, moving from 150mm SiC devices to 200mm SiC devices, thereby enabling a more energy efficient process with higher power density and higher operating temperature. The development of these chips will take place in a fully automated fab, which will also constitute a breakthrough innovation compared to the existing global state-of-the-art.

Description related to the complementarity of the individual projects

(170) The Member States submit that the projects in WS-ACT are complementary because they provide a tight mesh between different projects covering the entire microelectronics and communication technologies value chain. The various collaborations plan to allow the advances made at each level of the value chain to be cumulated, in order to enable the development of downstream applications at the best technological level. Novel materials and substrates are expected to be smartly integrated into semiconductor technologies and advanced packaging; themselves combined into novel components such as power modules and then into energy efficient sub-systems and systems that meet both the IPCEI ME/CT objectives, as well as the requirements of the downstream applications, notably the automotive sector.

(171) The complementarity character of the individual projects is illustrated by a number of collaborations within the WS, as explained in section 2.4.7.1.

*2.4.5. Description related to the significant added value and complementarity of the individual projects for the achievement of the goals of WS – COMMUNICATE*

(172) WS-COMMUNICATE is divided into four main WP and involves 24 participating undertakings, namely ADVA, Airbus, AVL, Codasip, Continium, Cogninn, Ericsson, FCM, GF, IFX-DE, IRVI, KDPOF, MEMC, Nokia (Nokia-DE and Nokia-FI), NXP (NXP-DE, NXP-NL and NXP-RO), Orange, R&S, SIAE, Soitec, STM (STM-FR and STM-IT), Trumpf Photonic, UMS, Wacker, X-FAB (X-FAB-DE and X-FAB-FR).

(173) The individual projects of the participating undertakings in this WS aim at carrying out innovative activities, aiming towards providing a significant added value to the development of microelectronic and communication technologies, which relate to the receipt and transmission of information from and to electronic equipment.

(174) WP 1 concerns the development of new innovative EDA tools for advanced node and high-frequency chips, as well as the development of advanced substrate materials, simulation tools and semiconductor equipment. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing multiphysics simulation and EDA tools for RISC-V based accelerator IP design with special attention to be paid on the co-design possibilities of the AI/ML high-performance ultra-low-power consumption solutions;

b) developing technologies operating in mmW frequency bands, thereby enabling conducted and over-the-air measurements beyond existing capabilities;

c) developing advanced materials for RF supporting the 5G – and subsequently the 6G – specifications, serving new diverse applications that require increase in frequencies. This task also includes the development of advanced substrates for photonics, which are expected to enable a further increase of the optical link transmission rates, while reducing energy consumption in next generation data centres; and

d) designing devices for 5G/6G application with the use of polysilicon raw material, which aims at supporting the development of the advanced substrates.

(175) WP 2 concerns the development of of semiconductor technologies, smart manufacturing, packaging and testing. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing photonics technology with robust design and functionalities for higher data at lower power consumption. This task also contains activities that aim at enhancing the system performance by a higher level of optimised integration of the various photonics and electronics platforms;

b) developing GaN and other III-V related RF technologies and materials (e.g., substrates and epitaxial wafer) and implementation of measurement and validation techniques;

c) advancing CMOS technologies for improved performance and power consumption to meet next generation wireless system and semiconductor requirements. This tasks furthermore contains activities that aim at developing advanced piezoelectric materials and processes for novel micro-acoustic filters for surface acoustic wave ("SAW") RF components for 5G/6G application;

d) developing advanced micro-acoustic filters for SAW components for 5G/6G application, using advanced materials and substrates for thin film deposition;

e) developing advanced packaging technologies by combining heterogeneous building blocks for application in components and (sub-) systems, such as radio front-ends and optical transceivers; and

f) developing innovative automation equipment, measurements techniques, and back-end assembly and test processes, aiming at improving quality and speed, while at the same time being cost efficient.

(176) WP 3 concerns the development of components and modules. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing radio and digital signal processing with algorithms, IP blocs and SoC solutions for 5G/6G communication systems and WiFi7 frequency bands;

b) designing analog to digital ("ADC") and digital to analog converters ("DAC") for complex, multi-channel, highly integrated optical and radio communication infrastructure systems (e.g., base station and cloud servers), which require higher resolution and communication data rate;

c) developing high-performing, energy-efficient, and secure processors and SoC devices and chipsets for 5G/6G and edge-AI communication systems, aiming at increasing AI/ML knowledge;

d) designing and developing RF components based on GaN technology, and power efficient, wideband RF components for 5G/6G applications and WiFi7 frequency bands; and

e) guaranteeing secure hardware products by developing on cyber security and IoT.

(177) WP 4 concerns the development of (sub-) systems for communication networks. The respective R&D&I and FID phases contain the following indicative tasks:

a) developing (sub-) systems for optical communications application that comprise highly integrated, advanced photonic and electro-optical components;

b) developing wireless transceivers for future radio systems in communication networks;

c) combining SW with HW design, thereby enabling the effective implementation of secure communication solutions with higher performance and lower power consumption;

d) designing end to end communication solution networks (i.e., terrestrial, radio, optical and satellite), enabling the virtualisation of HW and interoperable interfaces for communication systems that require high-performance processors, SW integration, energy efficiency and security;

e) providing reliable, smart and secure end-user terminals, as standalone devices and modular building blocks for device integration, such as in IoT or for mobility applications; and

f) developing edge-cloud and edge-AI solutions to provide safe and secure data processing and automation close to the data source, with the aim to enable the design of reliable IoT ecosystems.

Description related to the significant added value of the individual projects

ADVA

(178) ADVA's project aims at developing new coherent optical transceivers through highly automated and standardised assembly of microelectronics and Si photonics chiplets on a common substrate. In particular, ADVA will develop transceivers for high-bandwidth and high data communication rates, featuring superior optical signal to noise ratio ("OSNR"), while at the same time being energy efficient. These features will benefit several fields such as network monitoring, test and measurement equipment, optical satellite communications, 6G radio communications, HPC, quantum communications, fibre sensing and coherence tomography.

Airbus

(179) Airbus will develop […] 5G […] applications, namely: the 'tactical mobile node', […]; a 5G […] solution designed for helicopter communications; a 'naval communication node' for maritime applications; […] and […] aircraft solution. All of these […] applications are expected to contribute to solving the […] problems of existing 5G solutions, provide and enhanced coverage and improve their power efficiency.

AVL

(180) AVL's project will focus on the validation, qualification and optimisation of a cyber security system in vehicles. In particular, AVL aims at providing a crucial bridge between chip developers and car manufacturers by automatically generating models of the vehicle's HW/SW architecture and identifying vulnerabilities in this architecture, thereby increasing the test coverage and reducing the test time.

Codasip

(181) Codasip plans to develop more automated approaches in EDA tools through the development of RISC-V accelerator/digital signal processing for radio communication. The project plans to focus on AI/ML architecture for 5G/6G, notably vector engines, with improved and innovative memory subsystem, aiming towards achieving ultra-low-power consumption and higher data throughput.

Cogninn

(182) Cogninn's main objective is to develop a virtualized O-RAN ("vORAN") technologies towards the 6G-communication system and integrate AI enabling technologies that combine computing with networking. Cogninn will contribute to achieving the objectives of the WS by providing an open and disaggregated network, driven by open interface; by achieving programmability of the system that is distributed into different HW platforms; by allowing operators to select any vendor of any network domain; and by providing different vertical communication services within one vORAN.

Continium

(183) Continium's project aims at advancing the performance of analogue electronics design for analogue circuits, such as ADC or DAC. As a result, the project is expected to deliver the next generation technology of wireless base station transceiver system ("BTS"), with the aim at saving costs (i.e., lower chip manufacturing cost per unit due to lower chip area), reducing the energy consumption of ADC semiconductors and improving signal quality in wireless receivers.

Ericsson

(184) Ericsson's project aims at developing innovative microelectronic devices for 6G advanced antenna systems ("AAS"). In particular, Ericsson will conduct research on energy efficient GaN power amplifiers for 6G wireless communication networks, AD and DA data converters, low-power radio algorithms, packaging and analog front-end modules, thereby contributing to the objectives of the WS with the development of a disruptive digital radio chip technology, which is expected to display significantly better energy efficiency (up to 40%) and new 6G frequency bands.

FCM

(185) FCM's project aims at the development of high performance III-V-semiconductor substrates focusing on InP substrate wafer from 3"/4" (state-of-the-art) to 6" for fiber-optic and RF transceivers. Specific work objectives of the project concern the development and adaptation of the manufacturing technology (crystal growth, wafering), including the establishment of a pilot line, for larger substrate diameters and the achievement of a wafer quality suitable for the targeted applications.

GF

(186) GF plans to develop multiple next generation devices, such as microprocessors, mobile application processors, baseband processors, network processors, RF modems, microcontrollers, as well as power management units, display drivers and image signal processing ("ISP"). GF furthermore intends to establish techniques for the assembly and interconnection of all of these multiple devices in a single package.

The development of these devices is expected to enable the further development of high-performance, secure, and energy-efficient semiconductor chips with next-level RF capabilities (>100 GHz) for next generation 5G/6G digital communication systems.

IFX-DE

(187) IFX-DE will develop […] bipolar CMOS ("BiCMOS") technology, including assembly and packaging for automotive, radar, sensing and communication applications, […]. The project will also encompass the development of new RF components for future wireless infrastructures and high-frequency technology […] in future wireless communication, resulting in increased performance on data transfer, in reduced power consumption and higher level of heterogenous integration.

IRVI

(188) IRVI plans to provide start-ups and SMEs, with a portfolio of ultra-low-power consumption building blocks (e.g., memory, AI and information blocks, ADC/ACD design, off-the-shelf antenna solutions, edge-computing etc.), thereby supporting them in the development of their own SoC for IoT applications. This is planned to be carried in a new automated assembly, packaging and testing facility, whereby the start-ups and SMEs will test the required building blocks, with the aim to establishing prototyping IoT related products.

KDPOF

(189) KDPOF plans to develop a completely new concept for fiber optic transceiver, based on a single-chip optoelectronic component, addressing low-cost, high volume optoelectronics manufacturing and the design of the next generation of products enabling optical links for automotive applications. This next generation of products is expected to support a higher speed up to 25Gb/s and meet environmental and reliability requirements, for instance targeting specific temperature ranges.

MEMC

(190) MEMC's project aims to develop Si wafers characterised by very low contamination and scalability (200mm and 300mm), with the purpose of enabling further integration in the most advanced platforms. RF technologies in the multi-mmW band would benefit from the ultrapure Si wafers with very high substrate resistivity values (> thousands of Ohmcm) developed by MEMC, which are expected to minimise RF losses, cross-talk non-linearity, and ensure very low contamination.

Nokia-DE

(191) Nokia-DE's project intends to develop SW/HW solutions for high-speed optical networks and advanced mobile networks (5G/6G), including embedded edge-cloud and edge-AI solutions. In particular, Nokia-DE plans to develop a new generation of SoC devices, new radio network products based on the architecture and design of the SoC devices, including the corresponding SW/HW, and new optical network products, with the aim of supporting foundries with technology nodes down to 3 nm for higher performance and lower power consumption.

Nokia-FI

(192) Nokia-FI's project aims at strengthening networks systems chip design skills for advanced SoC radio access, edge-processing components, and ML/AI technologies for 5G/6G communication systems, both for consumer broadband communications and industry digitalisation. In particular, Nokia-FI's project will address a new type of computing-in-memory ("CiM") architecture for beyond the global state-of-the-art performance and power consumption, and develop new system chipset integration for high-performance architecture, thereby enabling digital radio front end and baseband solutions.

NXP-DE

(193) NXP-DE plans to establish a development centre for 5G/6G/WiFi/radar IP to design and develop - beyond 5G and 6G - IP and components required for enabling next generation mobile telecommunications networks, thereby offering high-security, high-bandwidth and low-latency services, regardless of the generation of radio technology, while leveraging use cases such as localisation and radar.

NXP-NL

(194) NXP-NL plans to establish a development centre for 5G/6G and beyond, as well as infrastructure for a mobile telecommunications network that offers high-bandwidth, low-latency services radio technology, ultra-low-power technology, cybersecurity, while enabling use cases, such as localisation and radar. The project aims at developing innovative RF module components, which can serve the low noise receive functions and drive the high-power transmit systems.

NXP-RO

(195) NXP-RO plans SW development kit packages for accelerator IPs, functional safety and security frameworks, integrated with industry leading infrastructure middleware and operating system solutions running on NXP-RO's baseband compute chip in ≤5nm technology. This is expected to provide high security, high bandwidth, low latency services and low-power connectivity, as well as meet the challenges of future cybersecurity with the implementation of post-quantum cryptographic capabilities.

Orange

(196) Orange's project aims at addressing the challenges of network virtualisation, enabled by SW and new HW that requires a complete redesign of the network functions. To this end, Orange will focus in the areas of ORAN, transport network, cooperative connected and automated mobility ("CCAM"), and private 5G, in order to develop flexible, secure and low impact networks with advanced features and services, thereby allowing for an integrated innovation approach to digital communications from SW to HW.

R&S

(197) The 6G network is expected to expand the 5G frequency range in the mmW region up to 170 GHz, while state-of-the-art broadband test and measurement solutions are currently limited to maximum 110 GHz. R&S project will develop and offer mmW T&M equipment operable up to 170 GHz. This equipment is crucial for research,

development and production of RF components for many applications in the microelectronic industry, not only next generation of mobile communication but also sensors, automotive radar, gesture recognition, material science, IoT and Industry 4.0.

SIAE

(198) SIAE's project aims at developing ASIC, RF devices and antennas for the setting up of a next generation wireless transport equipment (i.e., the transport layer, usually defined as backhaul, which connects the radio access tier to the infrastructure of the mobile service provider). As a result, the project is expected to support multiple configurations in order to carry the traffic of next 5G and 6G networks, and of an open radio unit ("O-RU") for open radio access network ("O-RAN") infrastructure, aimed at the modularisation and standardisation of radio network functions and interoperability between products.

Soitec

(199) Soitec will develop a new piezoelectric-on-insulator ("POI") wafer technology for RF filters aiming towards contributing to a decrease in the power consumption of RF filters. More precisely, Soitec will develop a 200mm diameter substrate, which is expected to allow 80% more filters to be made than on the existing 150mm substrate and will help standardise POI based RF filters for 5G sub-6 GHz, thereby contributing to the decrease in power consumption. In addition, Soitec aims at developing a lithium niobate ("LNO") based substrate in addition to the first generation based on lithium tantalate ("LTO"), addressing the new 5G bands between 2.5 GHz and 6 GHz.

STM-FR

(200) STM-FR's contribution to this WS lies in the development of dedicated components related to equipment and infrastructure for communication, radar and space applications. In particular, STM-FR plans to develop a new generation of BiCMOS, RF-SOI, FD-SOI RF technologies, in order to meet 5G mmW requirements, a new generation of RF filters based on integrated passive device or acoustic technologies, a 150 mm RF GaN on Si technology for communication infrastructure, and a RF module (SiP) technology.

STM-IT

(201) STM-IT's project aims at developing RF-MEMS and future RF modules operating in mmWave range and beyond based on new piezo materials. Furthermore, the project will focus on a new family of smart power devices to support powerline communication IC, as well as on mixed digital ASICs for communication devices, and on the development of next generation RF GaN HEMTs on silicon wafer with proprietary epitaxy. Finally, STM-IT's project plans to develop new functionalities in terms of security of embedded SIM in demanding environments, such as near the engine of a car or on a power meter.

Trumpf Photonic

(202) Trumpf Photonic's project aims at advancing the performance of VCSEL to enable next generation data and communications, thereby driving innovation in new

manufacturing processes, new modelling and material properties. In particular, the project will build on existing performance of VCSEL technology and is planned to go beyond the global state-of-the-art addressing the first products for the 100Gb/s market by advancing basic VCSEL performance with the use of new materials and device architectures, by integrating more system functionality into the VCSEL chip and by expanding the wavelength range of VCSEL towards 1300nm-1500nm, or higher.

UMS

(203) UMS's project aims at the development of a highly performant GaN-on-SiC technology for high-power telecom applications, in particular amplifiers, in a higher frequency up to 100GHz compared to the current state-of-the-art. In order to achieve adequate power efficiency at such high frequencies, UMS plans to optimise the GaN-on-Sic technology for modern integration, introducing substantial changes to the technology approach (e.g., epitaxial layer sequence, ohmic contacts, gate metals, passivation, device protection and contacting), thereby achieving the best possible process reproducibility and highest wafer yield.

Wacker

(204) Wacker's project aims at providing a next level polysilicon material for the development of new technologies in the downstream value chain, notably in 5G/6G high frequency filter devices. In particular, Wacker plans to develop polysilicon as an essential feedstock for 5G/6G applications, and lead to the next levels of purity, low contamination, and high resistivity, thereby enabling better performance of 5G/6G high frequency filter devices and avoiding signal loss.

X-FAB-DE

(205) X-FAB-DE will develop and implement novel wafer-level technologies for heterogeneous and 3D integration of microdevices and components, including ASICs, sensors and actuators, wide bandgap devices and photonic components. The project will have a technical focus on micro-transfer-printing ("MTP") and through-silicon-via ("TSV") technologies. The sensors and actuators developed will be integrated into the smart sensor systems of various applications (e.g., automotive, medical etc.). The heterogeneous integration using chiplet technology will be offered in a wide range of applications and 3D connection for combination of various devices will be available on a newly established foundry business model.

X-FAB-FR

(206) X-FAB-FR will develop an innovative method of multi-technology chip level integration of highly capable RF technologies, targeting 5G mmW/6G applications. This will entail the development of wide bandgap semiconductor materials like GaN, delivering high signal power at mmW frequencies, as well as the development of dedicated photonic IC for coherent optical communication. These developments aim towards addressing the requirements of 5G/6G autonomous vehicles and of integrated optics and photonics for new semiconductor technologies, which offer a higher data communication rate, while at the same time contributing to energy efficiency.

Description related to the complementarity of the individual projects

(207) According to the Member States, the individual projects in this WS are complementary because they are covering different segments in the microelectronic and communication technologies value chain. The planned innovations in materials, tools and substrates are expected to allow the advancement of technological processes on which functional blocks (i.e., IP) subsystems and systems will be designed. The different chip technologies developed in WS-COMMUNICATE could not be used efficiently in novel communication systems, notably 5G/6G and other wireless and optical communication networks, without the parallel evolution of adequate heterogeneous integration techniques that are also pursued in the WS. As a result, it is expected that the outcome stemming from the complementary individual projects will improve the performance of optical communication systems, wireless networks, as well as communication systems by satellite, and contribute to fulfilling the WS-COMMUNICATE's objectives.

(208) The complementarity character of the individual projects is illustrated by a number of collaborations within the WS, as explained in section 2.4.7.1.

### *2.4.6. Description related to the significant added value and complementarity between the WS for the achievement of the objectives of IPCEI ME/CT*

(209) The Member States submit that each of the four WS significantly add value to and is complementary with each other to meet the objectives of IPCEI ME/CT (see recital (10)).

(210) The figure below shows a schematic representation of the cross-border collaborative interactions between the participating undertakings contributing to the different WS of IPCEI ME/CT:

***Figure 3: Schematic representation of collaborations envisaged in IPCEI ME/CT***

#### 2.4.6.1. Description related to the significant added value of WS-SENSE and its complementarity with other WS

(211) WS-SENSE significantly adds value to the whole semiconductor industry thanks to the implementation of sensors needed to improve the manufacturing in semiconductor fabs. With the improved capacity to perform analytic in-line measurement of critical parameters, sensors are expected to contribute to implementing new technological and organisational measures in favour of a more efficient and greener manufacturing. In particular:

- Significant added value of WS-SENSE for the completion of WS-THINK: The implementation of processing capacities, such as AI/ML, into or close to the sensors will change the architectures of systems, thereby reducing processing and power consumption needs. This significant benefit of WS-SENSE to the completion of WS THINK can be illustrated thanks to the electrical architecture of highly automated driving ("HAD") vehicles, which relies on smart sensors to reduce the processing needs of central processors.

- Significant added value of WS-SENSE for the completion of WS-ACT: Electrical systems that will use technologies for power conversion developed in the WS-ACT will benefit from sensors enabling an improved battery management developed in the WS-SENSE.

- Significant added value of WS-SENSE for the completion of WS-COMMUNICATE: The use of larger wafers generally contributes to the industrial performance of a technology. For instance, the development of III-V materials for infrared sensors needed for the development of wafers for radio communication, illustrates the added value of WS-SENSE to the completion of WS-COMMUNICATE. Furthermore, the integration of optical emitters and sensors is compulsory for the development of powerful and energy-efficient advanced optical communications.

(212) Concerning the complementarity with other WS:

- WS-SENSE is complementary to WS-THINK: the joint design of sensors and processors in WS-SENSE opens new technological perspectives, offering the possibility to integrate AI features in sensors or cybersecurity features that are part of WS-THINK.

- WS-SENSE is complementary to WS-ACT: While the implementation of sensors contributes to develop packaging technologies enabling to follow the More-than-Moore technological trend, the use of new wide banggap technologies in WS-ACT will contribute to develop new encapsulation principles that will be compatible with more stringent conditions or requirements, such as voltage, temperature and reliability (e.g., the deployment of SiC technology under WS-ACT is expected to generate new technological solutions for the integration of sensors developed in WS-SENSE).

- WS-SENSE is complementary to WS-COMMUNICATE: The complementarity of WS-SENSE and WS-COMMUNICATE manifests itself in sensor components that integrate communication features, in order to enable the transfer of acquired data (e.g., integration of IoT communication modules into sensor modules, as part of a single SiP.

#### 2.4.6.2. Description related to the significant added value of WS-THINK and its complementarity with other WS

(213) WS–THINK leads to the development of advanced technology nodes, aiming at significantly adding value to the development of manufacturing and characterization equipment and testing methods, in terms of sensitivity, spatial resolution and accuracy. In particular:

- Significant added value of WS-THINK for the completion of WS-SENSE: the combination of robust technologies of WS-THINK, such as reliable digital technology node and non-volatile memories, in sensor modules of WS – SENSE, will enable the fast implementation of new features, which are expected to contribute at opening new perspectives, such as the development of edge-AI, to the applications of WS – SENSE (e.g., the FD-SOI technology used in automotive applications will aim at contributing towards a faster implementation of advanced radars).

- Significant added value of WS-THINK for the completion of WS-ACT: the integration technologies developed for the digital nodes in WS–THINK will be applied to the technologies developed in WS–ACT (e.g., the development of smart pixels in WS–THINK using microLED from WS–ACT is expected to add important benefits to the microLED technology itself).

- Significant added value of WS-THINK for the completion of WS-COMMUNICATE: WS-THINK will enable WS–COMMUNICATE to develop SW-defined and versatile components for RF communications (e.g., O-RAN solutions). Therefore, WS-COMMUNICATE is expected to benefit from the technological developments at wafer level in WS-THINK, and enable the development of ADCs and DACs, which are suited for future 6G applications.

(214) Concerning the complementarity with other WS:

- WS-THINK is complementary to WS-SENSE: While the development of WS-THINK often relies on technology development targeting smaller nodes (i.e., “More Moore”), WS-SENSE will contribute to the development of technologies that are valid for “More-than-Moore” (e.g., the development under WS – THINK of SiP based on organic substrates, with the use of components stemming from WS -SENSE).

- WS-THINK is complementary to WS-ACT: the packaging solutions obtained in WS ACT offer more robustness (e.g., voltage and thermal dissipation), while the ones used for WS-THINK generally offer accuracy and reproducibility at a large-scale. Furthermore, at wafer level, the high purity requirements generally needed for the Si substrates in WS-THINK are expected to benefit the Si power devices developed and in WS-ACT.

- WS-THINK is complementary to WS-COMMUNICATE: this complementarity can be seen for instance in the combination of digital conversion and emission reception features of WS–COMMUNICATE with cybersecurity technologies of WS–THINK (e.g., cybersecurity solutions in automotive connectivity applications).

2.4.6.3. Description related to the significant added value of WS – ACT and its complementarity with other WS

(215) WS-ACT will contribute to develop reliability models for defining failure mechanisms at semiconductor level. This reliability requirement directly derives from the final use of wide bandgap components in EV, which combines a high level of requirements (e.g., temperature range reliability, operating voltages etc.) with a long-term use of the product (e.g., during charging periods and driving). The acquired know-how is expected to benefit the entire semiconductor ecosystem. In particular:

- Significant added value of WS-ACT for the completion of WS-SENSE: the adoption of EV is expected to steer the need for sensors needed for AD, (e.g., the development of LiDAR in WS – SENSE based on GaN wafers in WS-ACT).

- Significant added value of WS-ACT for the completion of WS-THINK: WS-ACT will contribute to create new applications for the technologies developed in WS-THINK. For instance, AD solutions will require the fast processing of data (e.g., sensor fusion or AI/ML) arising from the various embedded sensors (e.g., LiDAR, radar, camera etc.) of microprocessors and/or microcontrollers developed in WS-THINK. Furthermore, the development of next generation power amplifiers within WS-ACT will be used for the development of more accurate and higher speed positioning of wafers and other modules in EUV lithography tools developed in WS-THINK.

- Significant added value of WS-ACT for the completion of WS-COMMUNICATE: WS-ACT will contribute to deploy wide bandgap technologies on large wafers (up to 300 mm), while the WS-COMMUNICATE, which adopts similar material and technologies (i.e., GaN), will benefit from the wide bandgap deployment, either in the form of pure material wafer or in the form of GaN on SOI or GaN on Si-based technologies.

(216) Concerning the complementarity with other WS:

- WS-ACT is complementary to WS-SENSE: while WS-ACT is mainly driven by the implementation of wide bandgap technologies that are compatible with high voltage operations, WS-SENSE mainly focuses on the ability to improve the spectrum of detection, through sensitivity (e.g., digital circuit technologies developed in WS–ACT will enable the integration of readout IC technology with infrared sensors (with stringent operating conditions and very high sensitivity requirements) in WS-SENSE.

- WS-ACT is complementary to WS-THINK: the technologies developed in WS-ACT are generally needed in harsh environmental conditions, while those developed in WS-THINK often focus on state-of-the-art and advanced nodes and integration technologies, which are not compatible with such conditions. This complementarity can be illustrated by the fact that leading edge-technologies are often adopted in condition-specific sectors once the use on specific applications is obtained.

- WS-ACT is complementary to WS-COMMUNICATE: The complementarity of WS-ACT with WS-COMMUNICATE mainly comes from the different

performances of the technologies developed in each WS. For instance, since III-V semiconductor components are vital for all upcoming technological disruptions in communication (5G/6G, IoT), both WSs use III-V-based materials, in order to reach high efficiency. However, WS-ACT will mainly target power applications (i.e., high voltages, high current), while for WS-COMMUNICATE the bandwidth and RF gain will be optimised.

2.4.6.4. Description related to the significant added value of WS – COMMUNICATE and its complementarity with other WS

(217) WS – COMMUNICATE value to the completion of the three other WS as it will contribute to develop enabling technologies in the connectivity domain. First, the integration of connected sensors for the supervision of semiconductor fabs is envisaged to improve the organisational efficiency of the manufacturing lines: the capacity to widely deploy low-power IoT capable devices in production lines is expected to generate production gains and a lower energy and water consumption. Furthermore, the deployment of 5G technologies is compulsory in various application domains, thereby contributing to the wide deployment of the technologies developed in the other WS. In particular:

- Significant added value of WS–COMMUNICATE for the completion of WS-SENSE: WS COMMUNICATE will offer a common technological base for the development of III-V materials and contribute to their implementation on Si substrates. Both WS use GaN and Indium Phosphide ("InP") components, which can be integrated on larger wafer diameters for the development of optical sensors, notably LiDAR. The heterogeneous integration technologies developed in WS–COMMUNICATE is expected thus to benefit technologies developed in WS–SENSE.

- Significant added value of WS–COMMUNICATE for the completion of WS-THINK: the high data transfer technologies and their integration into components developed in the frame of the WS-COMMUNICATE is expected to contribute to the development of "More Moore" solutions that are beneficial to the implementation of technologies developed in WS–THINK (e.g., the heterogeneous integration of communication technologies with processors).

- Significant added value of WS – COMMUNICATE for the completion of WS-ACT: a specific contribution of WS-COMMUNICATE for the completion of WS-ACT lies on the use of passive components. Indeed, passive components developed for signal filtering in WS-COMMUNICATE may find application in converters developed in WS-ACT, overcoming thus, electromagnetic compatibility issues generated by higher switching frequencies.

(218) Concerning the complementarity with other WS:

- WS–COMMUNICATE is complementary to WS-SENSE: The complementarity of WS-COMMUNICATE and WS-SENSE is illustrated in the application domains of similar materials. For instance, in WS-SENSE, the developed solutions are based on the capacity of materials to convert and amplify external signals, while in WS-COMMUNICATE, the frequency performances constitute the key element.

- WS-COMMUNICATE is complementary to WS-THINK: most of the technologies developed in WS-THINK are expected to find complementary use in data transmission devices of WS-COMMUNICATE. The integration in single SiP of advanced processing devices, such as FPGA, together with broadband data converters illustrates this functional complementarity. This complementarity is equally challenging at substrate level: for instance, high resistivity carrier wafers developed in WS–THINK are needed for effective RF performances in WS–COMMUNICATE, and accordingly for the co-integration of functions in a single chip.

- WS-COMMUNICATE is complementary to WS–ACT: while III-V technologies and their integration (e.g., packaging) developed in WS-COMMUNICATE focus on the performances in the frequency domain, WS-ACT may use similar materials but in different operating conditions, which imply, for instance, different failure mechanisms. This complementarity of the application domain is expected to reinforce the overall knowledge of materials and the associated failure modes and effects.

(219) The significant added value and complementarity is illustrated in particular by the multiple collaborations between the participating undertakings contributing in the different WS, as described in section 2.4.7.2.

### *2.4.7. Collaborations within IPCEI ME/CT with respect to the relevant WS*

(220) In addition to the significant added value and complementarity of the individual projects within each WS, according to the information provided by the Member States, strong collaborations of the participating undertakings within and across the WS are planned, which, according to the Member States would not occur to the same extent and within the same time frame without IPCEI ME/CT.

#### 2.4.7.1. Examples of collaborations intra WS

(221) In WS-SENSE:

- Bosch-DE and NXP-AT will jointly work on ultra-low energy sensors, enabling energy efficient systems for industrial, mobile and IoT applications. Bosch-DE intends to provide IoT use cases and evaluate prototype and concepts, while NXP-AT will work on concepts and chipsets, allowing ultra-low energy systems.

- Osram will collaborate with NXP-NL on the development of sensor systems for ADAS. In particular, they will jointly work on the development of AI-based, SW-based and ultra-low-power sensors, whereby OSRAM will develop emitters for various wavelength and in adapted dimensions, and NXP-NL will contribute with the development of electronic components, advanced driving and operation SW for future sensors.

- Trumpf Photonic and Vigo will jointly work on the development of high-speed indium gallium arsenide (“InGaAs”) photodiodes. In particular, this collaboration will focus on co-developing the design, epitaxy and processing of high-speed InGaAs photodiodes, that will be combined with VCSELs and photodetectors.

- The collaboration between Mycroft and NXP-NL will enable the development of advanced ultra-low-power AI and modules for edge-computing. Mycroft and NXP-NL will focus on gap filling enablement of ultra-low-power AI technology. The cooperation foresees bringing this technology into existing and new use cases, including adaptive sensors to environment, energy grid specific use cases in metering and necessary MCU configuration optimisations options and accelerators. Metrics and benchmarking will be provided from Mycroft on selected NXP-NL's MCU platforms targeting the use cases and objectives of NXP-NL's project.

- Wacker and MEMC will jointly work on the development of high purity polysilicon to be utilised for high performing 200mm and 300mm wafers targeting highly advanced CMOS image sensor applications. MEMC will optimise its processes for utilising this newly developed high purity polysilicon to produce 200mm and 300mm advanced Si wafers and will test all wafers contamination characteristics to guarantee that they will respect the agreed specifications and the most advanced metal and lifetime standards. Wacker plans to develop the new and advanced polysilicon and will optimise its process based on MEMC's feedback.

- AVL and Bosch-RO will jointly work on the development of validation concepts for future ADAS/AD sensors. AVL will evaluate advanced testing tools for verification and validation of future on-board ADAS/AD sensors (e.g., LiDAR, radar, video), which are to be developed and produced by Bosch-RO.

(222) In WS-THINK:

- Codasip and Elmos have agreed to collaborate with the purpose of developing a prototyping platform with energy-efficient high-performance fully customisable RISC-V processor, with extensions for AI/ML and security solutions for automotive applications. Elmos will provide the specifications for a RICS-V development environment, as well as the automotive requirements concerning functional safety and cyber security, while Codasip will assist Elmos to integrate RISC-V technology into the latter's environment.

- The cooperation between Nearfield and BLK aims at combining Nearfield's 3D full die ("3DFD") dimensional metrology solution with characterisation techniques, […]. BLK will deliver wafers for system development and Nearfield will develop the 3DFD inspection and metrology system.

- The collaboration between Codasip and NXP-RO will enable the development of EDA tool extensions for HPC and high-performance RISC-V IP automotive SW. Codasip will develop the security features modelling in the EDA tool, while NXP-RO will benefit from a hardened RISC-V toolset for automotive quality requirements.

- […] and STM-MT will jointly work on an application of energy grid aware AI/ML data analytics and tools to enable energy saving on the advanced back-end manufacturing facility of STM-MT. STM-MT will provide the production sensor and monitor data and infrastructure, while […] will develop and deliver the tailored smart factory solution utilising its AI/ML products and know-how.

- The collaboration between STM-FR and Thermo Fisher is expected to improve the transmission electron microscopy ("TEM") workflow productivity and accelerate the development of new semiconductor devices. Thermo Fisher will develop and deploy new SW to increase the productivity of the TEM workflow tools at STM-FR, while the latter will test and evaluate the SW in the TEM characterisation steps during development of new devices, such as advanced flash memories and innovative micro-controllers.

- X-FAB-FR and Sunlight will collaborate on the development of new solutions for BMS, notably the development of low-power specific A/D sensors and interfaces targeting smart BMS. X-FAB-FR will develop and optimise its sensor technology for the smart battery management by realising specific product design kits ("PDK") and IC prototypes, while Sunlight will integrate and test the IC prototypes in its battery prototypes.

- NXP-DE and Bosch-RO will collaborate on the development of next generation automotive systems. The collaboration will include the joint design and development of next generation automotive systems through early sharing of information and feedback, that will allow the adaptation and tuning of the Bosch-RO's applications to NXP-DE's processors and associated SW.

- The cooperation between FMC and […] targets the development of FMC's technology for low-power and high-performance SoC applications with advanced nodes. […] will explore the integration capabilities of new materials generations, which will be developed by FMC, for new memories with new functions inside CMOS-based circuits.

(223) In WS-ACT:

- The collaboration between ZF and Renault will enable the development of a power electronics box […]. ZF will provide […] with the aim to conduct a joint optimisation […], while Renault will be involved as a downstream application user […].

- EEMCO will collaborate with STM-IT to develop new equipment for crystal growth for SiC technologies. STM-IT will work on the design and the development of a new generation of SiC components, while EEMCO will work on the development of a completely new model of single crystal growth equipment.

- The collaboration between Vitesco and STM-IT will enable the development of […] Wide Band Gap product solutions. STM-IT will support the development of […] and Vitesco will integrate and validate solutions for wide bandgap in power electronics automotive application […].

- MEMC and Aledia will jointly work on process development for the manufacturing of Si substrates of specific […] and the development of innovative micro-LED solutions. MEMC will develop new processes and provide the required wafers with the necessary characteristics for sustaining micro-LED solutions, while Aledia will provide feedback with all necessary test results and validation by processing the samples provided.

- Semikron-DE and Soitec have agreed to collaborate for the qualification of smart SiC advanced substrates for power modules and traction inverters for EV. Semikron-DE will characterise devices and power modules based on Soitec novel smart cut technology and develop a power module for EV vehicles traction inverted. Soitec will benchmark includes also benchmarking of SOITEC's smart SiC substrates with traditional SiC bulk approaches.

- Valeo and STM-IT will jointly work on the design and development of a new generation of WBG components. Valeo will focus on power modules, […] for automotive applications, while STM-IT will focus on the development of WBG power products […] to support future automotive electrification.

- […] and mi2 will collaborate on the application of high energy ion implantation and layer transfer technologies. Their collaboration will mainly focus on synergies between both technologies, and it is expected to provide benefits in terms of performance and energy efficiency.

(224) In WS-COMMUNICATE:

- Nokia-DE and […] will collaborate to jointly design ASICs for […]. […] will focus on broadband ADC digitisers while Nokia will implement digital signal processing in […].

- The collaboration between UMS and SIAE is expected to develop high-power amplifiers based on GaN-on-SiC technology. In particular, UMS intends to develop an advanced GaN-on-SiC technology for telecom applications, while SIAE will carry out successive refinements based on process yield, actual measured performances and design kit optimisations.

- The cooperation between R&S and Airbus will enable the development of 5G hybrid NTN test and measurement solutions. R&S will provide access to NTN test solutions and test and measurement equipment, while Airbus will validate the R&S's test solutions and provide feedback for further improvements.

- ADVA will collaborate with Orange on the integration of transceivers into mobile and terrestrial communication networks. ADVA will provide pluggable electro-optical transceivers, while Orange will test and integrate the transceivers in its white box optical transport and O-RAN testbeds.

- The collaboration between Codasip and Nokia-FI will enable the development of […] RISC-V accelerator for radio communication […] for 5GA/6G applications […].

- The collaboration between IRVI and Continium will enable the development of a high-performance chip with 5G connection to be used in IoT applications. Continium plans to provide data converters design and support in the design phase to enable the target specification definitions, technology analysis for low-power, high-performance and reliability, whereas IRVI will provide low-power consumption SoC.

#### 2.4.7.2. Examples of collaborations inter WS

(225) Concerning the collaborations between WS-SENSE and WS-THINK the following examples show the complementarity of the individual projects:

- Microelectronics parts and solutions developed by NXP-RO will be used by AVL to develop and manufacture test systems that include new validation methods in the automotive industry (e.g., ECU/DCU Security, ADAS/AD sensors, etc). NXP-RO will benefit from validation of the automotive processing solution under new use cases.

- The cooperation between Continental-RO and Bizzcom will enable the implementation of memristor/AI based solutions into smart sensors for automotive application, with an impact on chip and system architecture. The partners will share know-how and best practices in industrial automation, encapsulation principle, and technology design, development and implementation, in order to ensure that the memristor-based products meet the required standards and are seamlessly integrated into OEM solutions.

- The cooperation between Osram and Zeiss will enable analytic in-line measurements, aiming to improve energy efficiency. Zeiss will develop tools and methods for in-line analytics, designed lithographic optics, mask infrastructures, metrology of masks, mask repair and process control solutions, while Osram will conduct an analysis of the energy efficiency in semiconductor production along the full supply chain. The methods developed by Zeiss will be applied to and integrated in Osram's manufacturing processes.

(226) As regards the collaborations between WS-SENSE and WS-ACT:

- NXP-AT and Soitec will cooperate to enable energy efficient systems, focusing on achieving low-power solutions. Soitec will design innovative substrates for the manufacturing of high performance, low-power IC using FD-SOI technology, while NXP-AT will develop a next generation highly secure RISC-V processing platform and a next generation safe and secure BMS for EV.

- STM-IT and Semikron-SK will jointly work on the integration of new chip generation in power electronic modules and the increase in chip package power density, lifetime and reliability. STM-IT will provide new generation of SiC chips technologies and knowledge sharing, while Semikron-SK will perform activities with new SIC MOSFET chips generations, and evaluation in terms of production feasibility.

- Osram will collaborate with Semikron-DE on the development of advanced packaging between power and opto-semiconductors. Semikron-DE will provide the assembly of large arrays of compound semiconductors, while Osram will carry out testing for reliability and aging behavior of high-power packages and devices and their modelling.

(227) Concerning the collaborations between WS-SENSE and WS-COMMUNICATE:

- The collaboration between Trumpf Photonic and KDPOF will enable the development and qualification of a VCSEL and a photodiode for high-speed optical transceivers used in automotive applications. Trumpf Photonic will

develop and qualify a VCSEL and a photodiode, and KDPOF will integrate them into its optical transceiver for in-car communications.

- Osram and X-FAB-FR will collaborate on the hetero-integration of electronics and photonics' components for AD. Both undertakings will work on the joint integration of miniaturised opto-electronics, contributed by Osram, and customised memory chips and other electronics, contributed by X-FAB-FR.

- Bosch-DE and […] will jointly work on the implementation of 6G for connected mobility. Bosch-DE will work on a combination concept of sensing and radar for connected mobility, while […] will work on the 6G component integration and the identification of required semiconductor components.

(228) The complementarity between WS-THINK and WS-SENSE is also evidenced by a number of envisaged collaborations:

- Continental-FR and NXP-NL will jointly work on sensors for automotive applications and new modular HAD vehicle network platform with a focus on functional safety. Continental-FR will provide automotive context and electronic architecture variants required to support future automotive HPC needs, while NXP-NL will bring its expertise on smart sensors and impact on HAD systems.

- Semidynamics will collaborate with Menarini to design AI algorithms and provide HW acceleration to perform high-throughput single cell sorting from heterogeneous samples. Semidynamics will evaluate on its HW acceleration platforms real time performance of AI algorithms developed by Menarini.

- Mycroft and Elmos will collaborate on methods and solutions as to how to equip IoT and sensors with limited microcontroller resources with edge-AI and on-site ML features. Mycroft plans to explore the potential of energy models for edge-AI in EV and processing electricity measurements of battery readings, while Elmos will perform evaluations of the new generation of 3D environments.

(229) Concerning the collaborations between WS-THINK and WS-ACT:

- AT&S and Aledia will jointly work on the implementation of a packaging supply chain for advanced lower nodes down to 5/5nm. Aledia will focus on manufacturing of smart pixel technology, as well as CMOS devices for the microLED technology, while AT&S will focus on IC substrate for advanced packaging of HPC processors.

- STM-FR and MEMC will collaborate on the development of highly pure and engineered wafers for advanced sensors and logic/mixed signals applications. MEMC will focus on the development of advanced Si wafer substrates, while STM-FR will communicate to MEMC its requirements and specifications, to reach the desired performances associated with reliability and cost.

- The cooperation between Bizzcom and Semikron-SK targets technology exchange to achieve the common objective of innovative tailor-made complex solutions in the field of automation, robotics for serial production of power modules, and encapsulation. Semikron-SK will develop the packaging

processes, bonding and gluing technologies, while Bizzcom will focus on cooperation and development in the field of automation and robotisation of production processes, technical clean less solution, design, and development of power modules traceability solutions.

(230) Concerning the collaborations between WS-THINK and WS-COMMUNICATE:

- The collaboration between NXP-AT and R&S will advance new measurement and characterization equipment for high-frequency applications for UWB and RISC-V based solutions. R&S will modify its test and measurement equipment for NXP-AT's advanced UWB/radar and RISC-V developments.

- Openchip and Orange will jointly co-design SW and HW for high performance 5G/6G communication systems. The undertakings will identify 5G/6G communication infrastructure requirements for high performance computing solutions to support new network features and capabilities. Openchip will develop an accelerated use case proof of concept targeting 5G/6G edge-HPC and AI/ML use cases, while Orange will qualify the components, subsystem, HR and SW in terms of performance, energy efficiency and security.

- AT&S and Ericsson will collaborate to develop analog front-end modules ("AFM") for future 6G radios. AT&S will design, simulates and manufacture a substrate for an integrated analogue front-end ("AFE") multi chip module ("MCM") for future AAS radios, in the frequency range of 6-15 GHz developed by Ericsson.

(231) Concerning the collaborations between WS-ACT and WS-SENSE, the following examples show the complementarity of the individual projects:

- The collaboration between GF and […] will enable the development of chiplets and heterogeneous integrated products in the families of image processors, display drivers, radar and sensing technologies. GF will focus on the development of novel technologies for automotive technology platforms, while […] will focus on the implementation of GF technologies in its newly developed modules.

- The cooperation between Continental-FR and NXP-NL will enable the development of sensors for automotive applications and of a new modular HAD vehicle network platform with a focus on functional safety. Continental-FR will provide automotive context and electronic architecture variants required to support future automotive HPC needs, while NXP-NL will bring its expertise on smart sensors and impact on HAD systems.

- STM-FR and Continental-RO will jointly work on the integration of new photonic sensors in the automotive domain. STM-FR will provide newly developed photonic sensors for automotive safety, while Continental-RO will implement them in automotive architectures.

(232) Concerning the collaborations between WS-ACT and WS-THINK:

- ADI and ASML will jointly work on the development of a high-NA EUV technology, which requires more accurate and higher speed positioning of wafers and other modules in the ASML machines. ASML will focus on the development of deep ultraviolet ("DUV") lithography systems, while ADI will provide design and develop next generation precision amplifiers.

- The collaboration between IFX-AT and Mycroft targets the evaluation of various programmable SoC features to develop new embedded and specific AI modules for applications, such as energy grid management. The scope of the collaboration is on the feasibility and evaluation of the programmable SoC configurable platform, configuration evaluation and potential tools extensions. IFX-AT will provide the programmable SoC platform and Mycroft will develop autonomous low-power AI algorithms.
- ZF and ASML will jointly work on the development of manufacturing processes and application of Si processes to SiC (e.g., lithography). In particular, the undertakings will work on the enhancement of manufacturing process steps of WBG materials, which are more delicate and require more specific processing than Si, and on the export of the process technology knowhow from small node technologies to SiC.

(233) As regards the collaborations between WS-ACT and WS-COMMUNICATE:

- IFX-DE and […] will collaborate in the field of RF power amplifiers for 5G/6G mobile networks and rectifiers for power supplies. IFX-DE will deliver RF GaN transistors […], as well as power amplifier modules based on the RF GaN transistors, considering the specifications of […] for 5G/6G applications. […] on the other hand, will evaluate the modules for the said applications.

- The cooperation between FCM and UMS is expected to enable the development of GaN substrates ready for epitaxy for automotive and radar systems. FCM plans to develop a crystal growing process for free-standing GaN wafers, while UMS will use the GaN substrates for product development and production line qualification for advanced GaN e-band technologies.

(234) Concerning the collaborations between WS-COMMUNICATE and WS-SENSE, the following examples show the complementarity of the individual projects:

- The cooperation between KDPOF and Vigo will enable the development of epitaxial layers technology and enhanced III-V InP epitaxial process for automotive applications. In particular,KDPOF and Vigo will jointly work on the development of new integrated photonics fabrication technology according to automotive requirements and on mid-infrared photonic IC.

- X-FAB-DE and Lynred will collaborate regarding the development of advanced CMOS readout IC […] for the next generation of micro-bolometer sensors. […].

- R&S and NXP-NL will jointly work on new measurement and characterisation equipment for high frequency/millimeter wave testing. R&S will develop test and measurement equipment for NXP-NL's advanced radar development.

(235) Concerning the collaborations between WS-COMMUNICATE and WS-THINK:

- The collaboration between Nokia-FI and ASML will enable the development of […] lithography solutions for advanced node chips […] telecommunication devices. […]

- Cogninn and Tachyum will jointly work on the development of 5G O-RAN technology aiming for better energy consumption, network optimalisation and security powered by Tachyum's HPC/AI. Cogninn will prepare SW and HW tools for the integration of Tachyum's HPC/AI to its devices, while Tachyum will prepare SW libraries and tools for the integration of its HPC/AI to Cognitive innovations devices.

- The cooperation between R&S and Cologne Chip will concern projects for FPGA including AI. R&S will provide insights of future FPGA technical specifications and features, while Cologne Chip will deliver FPGA with AI for signal processing.

- IRVI and Teledyne will collaborate to develop SiP of advanced IoT circuits. Teledyne will offer its engineering skills and testing capabilities within the field of packaging technologies and SiP for the development of its IRVI's IoT device.

(236) As regards the collaborations between WS-COMMUNICATE and WS-ACT:

- The collaboration between FCM and SGL will enable the development, testing and qualification of advanced graphite parts for synthesis and crystal growing of InP boules. SGL will develop advanced graphite components for synthesis and crystal growth equipment of InP boules, while FCM will perform measurements and analysis of heat conductivity and heat flow during InP boules crystal growth.

- X-FAB-DE will jointly work with X-FAB-FR on MEMS-based and microfluidic systems and technologies to develop new photonic systems with unique performances. X-FAB-GER will work on the advancement of technologies for assembly and will interconnect micro-transfer-printing to combine passive SiN-based integrated photonic components developed by X-FAB-FR with active III-V components.

### 2.5. Positive spillover effects generated by IPCEI ME/CT

(237) The Member States submit that IPCEI ME/CT will generate important dissemination and spillover effects across the Union. This dissemination will be made possible through:

a. dissemination and spillover of results that are not protected by intellectual property ("IP") rights (see section 2.5.1);

b. dissemination and spillover of results that are protected by IP right (see section 2.5.2);

c. dissemination and spillover of results during the FID (see section 2.5.3);

d. dissemination and spillover of results to the associated participants (see section 2.5.4); and

e. dissemination and spillover of results to other indirect partners and to other sectors (see section 2.5.5).

(238) The individual projects notified as part of IPCEI ME/CT detail that each participating undertaking commits to and will participate in activities enabling dissemination and spillover effects up until, and including, the final eligible year of each individual project (see Table 21 under recital (329)). A member of the FG will be designated as key contact for the implementation of the dissemination and spillover commitments.

*2.5.1. Dissemination and spillover of results that are not protected by IP rights*

2.5.1.1. Overview of the dissemination and spillover strategy of non-IP-protected results

(239) The participating undertakings to IPCEI ME/CT commit to disseminate knowledge and the individual project results that are not protected by IP rights to the scientific community and the industry.

(240) The table below displays the mapping of the main dissemination actions of the non-IP protected results of IPCEI ME/CT within the Union:

| Event | Participating undertakings (examples) | Scope (examples) |
|---|---|---|
| **Conference/Meeting/Fair** | All participating undertakings | • Display technologies (European Technical Conference)<br>• Key partner conference with vendor partners<br>• Community conference on microelectronics |
| **Newsletters/Brochures** | Lynred, mi2, Sunlight, Teledyne, Valeo, X-FAB-FR, X-FAB-DE | • Internal communications on objectives and results<br>• External communications of achievements |
| **Open-Day/Site visits** | Aledia, Airbus, Bizzcom, SGL, MEMC, Teledyne, Lynred, Valeo, Vitesco | • AR innovation<br>• Plant anniversary celebration<br>• Facility visits<br>• Project progress, including virtual tours |
| **Press Release/Press Event** | Aledia, Bosch-RO, Continental-FR, Ericsson, IFX-DE, Lynred, mi2, Nokia-DE, Semikron-DE, SGL, Soitec, STM-FR, STM-IT, Teledyne, Valeo, Vitesco, Wacker, X-FAB-DE | • Status updates<br>• Information on projects and products<br>• Press releases on achievements and deliverables of the projects |
| **Roadshow** | ADVA, SGL, X-FAB-DE | • Presentation of technologies for different applications, exchange between the different actors of the related industry value chain<br>• Locally highlighting IPCEI efforts at local events<br>• Exhibition of transceiver samples, photonics wafers |

| | | |
|---|---|---|
| **Social Media** | Aledia, BLK, Bosch-DE, Bosch-RO, Continental-FR, Continium, Elmos, IFX-DE, MEMC, mi2, Nokia-DE, Osram, R&S, Semikron-DE, SGL, Soitec-FR, STM-FR, STM-IT, STM-MT, Teledyne, Trumpf Photonic, Valeo, Wacker, X-FAB-FR, X-FAB-GER, Zeiss | • Information on technical progress, milestones, spillover actions<br>• Newsletter on company's website presenting the results<br>• Publication of results on IEEE global spec |
| **Website** | Aledia, Bosch-DE, Cologne Chip, Elmos, IFX-DE, mi2, Nokia-DE, Orange, R&S, SGL, Trumpf Photonic, Valeo, X-FAB-DE, X-FAB-FR | • Publication of results through IPCEI ME/CT website and communication on events<br>• Publication of results on O-RAN website<br>• Data available on open access data base |
| **Webinars** | Airbus, AVL, Bizzcom, Codasip, Lynred, Soitec, Vigo, X-FAB-DE, X-FAB-FR, Sunlight, Zeiss | • Live demonstrations of IPCEI ME/CT results online<br>• Micro-transfer-printing technology, glass wafer processing platform |
| **Workshop/Seminar/Summer School** | ASML, AT&S, AVL, Bosch-DE Codasip, Cologne Chip, Continental-FR, Continium EEMCO, Elmos, Ericsson, GF, IFX-AT, IFX-DE, Mycroft, NXP-AT, NXP-DE, NXP-NL, R&S, Semikron-DE, SIAE, Soitec-FR STM-FR, STM-IT, STM-MT, Teledyne, Trumpf Photonic, Valeo, Vigo, Vitesco, Wacker, X-FAB-DE, X-FAB-FR, Zeiss, ZF | • Access to pilot lines<br>• Advantages of GaAs technology<br>• Smart power electronics enabling the green transition<br>• Biomedical applications<br>• Workshop on RISC-V components and processor architecture<br>• Dedicated workshop for SMEs and start-ups<br>• Workshop on wide bandgap power devices and applications<br>• Hackathon on SiC devices and digitalisation<br>• Innovation roundtable and technical wafer workshops<br>• Power electronics for downstream applications<br>• Future mobile communication industry trends |

***Table 2: Matrix of dissemination and spillover strategy of non-IP protected results***

(241) The following table details in a quantitative manner the main dissemination actions envisaged by the participating undertakings, as a result of the commitments made by the participating undertakings:

| Key performance indicators ("KPIs") | Expected dissemination in the course of IPCEI ME/CT (estimates over the course of the project) | Difference with "business as usual" (estimates over the course of the project) ([15]) |
|---|---|---|
| Industrial/Scientific publications | 1398 | +1258 |
| Participation in conferences (presentations, papers, exhibitor, etc.) | 1145 | +882 |
| Organiser of external events and company events for SMEs | 298 | +162 |
| Funding of PhD studies | 467 | +400 |
| Funding of master thesis | 569 | +427 |
| Internships | 662 | +662 |
| Financed university chairs | 65 | +45 |
| Patent generation | 2472 | +2089 |
| Research contracts with academia and Research Organizations ("RO") | 339 | +230 |
| Licensing to universities or ROs | 68 | +53 |
| Multi-Project Wafer promotion and design | 443 | +358 |
| Distribution of PDK | 1558 | +1558 |
| Joint Undertaking collaborations | 384 | +384 |

1. ***Table 3: KPIs for dissemination and spillover knowledge***

#### 2.5.1.2. Participation in external events

(242) The participating undertakings commit to participate in conferences and public presentations within the Union in the framework of international events listed in the following table, during which they will disseminate knowledge and the individual projects' results that are not protected by IP rights.

(243) These events will take place in multiple Member States, not only those participating in IPCEI ME/CT, including but not limited to the participating undertakings. They relate to a number of different sectors beyond the sector(s) where each participating undertaking operates. They are open to participants from all Union Member States and ensure wide geographic coverage, beyond the participating undertakings. A non-exhaustive list of conferences and events, where participating undertakings will present their work includes the following:

([15]) The Member States have requested from the participating undertakings to submit estimates of the number of dissemination actions that they carry out ordinarily (i.e., 'business as usual') and to compare them with the envisaged number of dissemination actions that the participating undertakings expect to carry out as part of the individual projects notified in IPCEI ME/CT.

| Conference Title, Location ([16]) | Participating undertakings | Main topics addressed (examples) |
|---|---|---|
| **5G Expo Europe** | AVL, Continium; NXP-RO, Orange | • Validation methods for secure chips used in architectures of Connected Vehicles<br>• O-RAN and software-defined communication systems in 5G/6G<br>• Wireless receiver based on Continuous-Time Sigma-Delta ADC |
| **International Conference on Electrical and Electronic technologies for Automotive** | ADI, AVL, NXP-RO, Soitec | • Application of magnetic sensors in the automotive sector<br>• Energy efficiency optimisation thanks to microelectronics solutions |
| **International Laser Technology Congress** | AT&S, Sunlight | Application of laser in the manufacturing processes of PCB and substrates |
| **Bordnetz Congress: Annual automotive connectivity fair, Germany** | AVL, Elmos, KDPOF | • Validation systems for energy-efficient power electronics for EV<br>• Innovative LiDAR solutions for automotive<br>• Gesture and ultrasonic sensors |
| **Compound Semiconductor International Conference** | AVL, IFX-AT, Soitec, Valeo | • The reliability of SiC power modules: presentation of endurance and qualification models and tests of devices<br>• Performances and reliability of dies assembly based on smart SiC process<br>• Evaluation results of 800V-power modules reliability and performances |
| **Conference on International Power Electronics Systems, Germany** | IFX-AT, MEMC, Soitec | • From devices to modules: the future of SiC<br>• Advanced Si wafers manufacturing for power electronics<br>• Device performance and reliability on smart SiC |
| **European Advanced Process Control and Manufacturing Conference (apc\|m)** | ADI, EEMCO, Elmos, IFX-AT, Valeo, X-FAB-FR | • Semiconductor manufacturing effectiveness and productivity<br>• Manufacturability of atomic layer oxide growth for high-performance bipolar devices<br>• Process control applied to Si photonics |
| **Electronic Based Systems Conference, Austria** | AVL, GF, IFX-AT, IFX-DE | • Automotive sensors and intelligent measurement and test systems<br>• Power electronis |
| **Embedded World, Germany** | AVL Codasip; Mycroft, NXP-RO | • Implementation of AI features in embedded systems<br>• Embedded radar solutions applied to automotive |
| **European Conference on Integrated Optics** | BLK, Bosch-DE, Vigo | Development of the integrated photonics platform for mid-infrared (hybrid/heterogeneous integration, graphene integrated photonics, |

([16]) If no location of an event is mentioned, the location is either changing each time, is online or not (yet) defined, etc.

| Conference Title, Location ([16]) | Participating undertakings | Main topics addressed (examples) |
|---|---|---|
| | | photonic IC, photonic building blocks, photonic transceivers, assembly, packaging techniques) |
| **European Conference on Optical Communication** | ADVA, AT&S, KDPOF, Soitec, Trumpf Photonic, X-FAB-FR | • Quantum key distribution<br>• Application of substrates on insulator technologies on Si photonics |
| **European Conference on Crystal Growth** | EEMCO | Crystal growth advanced processes applied to SiC manufacturing |
| **European Forum for Electronic Components and systems** | AVL, IFX-AT, BLK, FMC, NXP-AT, NXP-NL, NXP-RO, Osram, Teledyne, Valeo, X-FAB-FR | • Performances of ultra-small ferroelectric capacitors<br>• Performance demonstration of electronic components such as 6G antenna in package technology<br>• SiP based on organic flip-chip<br>• Graphene integrated photonics |
| **European Microelectronics and Packaging Conference and Exhibition** | Continental-RO, FCM, IRVI, KDPOF | • IoT 5G modules based on 3D heterogeneous integration of components |
| **European Microwave Week** | NXP-NL, Lynred, SIAE, Soitec, Teledyne, X-FAB-FR | • Circuit design and/or electromagnetic simulations of packages<br>• Hybridisation technology for the development of very large Infrared Focal Plane Arrays;<br>• Device performance using SmartCut POI substrates<br>• Advanced SiP targeting high-performances in RF data conversion<br>• Propagation and smart antennas for multi-band wireless transport at mm-wave frequencies<br>• Sensitive analysis of filter design based on stochastic method |
| **European Conference on Silicon Carbide and Related Materials** | EEMCO, IFX-AT, MEMC, SGL, Soitec, Vitesco | • Advanced Si wafers fabrication for new bipolar-CMOS-DMOS platforms<br>• Wide bandgap towards power electronic product benefits<br>• Performances of the SmartCut applied to SiC wafers |
| **ECSEL/KDT JU Symposium** | AVL, Cosasip, IFX-AT, NXP-RO, Openchip, STM-FR, STM-IT, STM-MT | • EDA tool extensions for advanced RISC-V core design<br>• IR and Bio-inspired MEMS<br>• New Digital and Memory nodes based on P18 technology<br>• Power GaN and SiC components<br>• 5G mmW technologies |
| **European Space Components** | Teledyne | RF data conversion requirement in Advanced Systems-in-Packages |
| **Eurosensor** | ADI, AVL, Sunlight | • Packaging architecture innovations<br>• Advanced sensor control for synthetic biology<br>• Optical sensors electronic readout circuits |
| **GaN Marathon** | IFX-AT | Application of GaN technology on devices for high and low-power |
| **German Oracle Users-** | Elmos | Data base architectures for functional |

| Conference Title, Location ([16]) | Participating undertakings | Main topics addressed (examples) |
|---|---|---|
| **Group, Germany** | | test data suited for data science |
| **German Physical Society Meetings, Germany** | Osram | • IR light sources for sensing applications<br>• Smart lighting and µLEDs<br>• Sustainable and Green UV-C light sources<br>• Intelligent and efficient headlamps |
| **Global Internet of Things Summit** | IRVI | • International conference established to attract and present cutting-edge research results on the IoT<br>• Topics: blockchain, IoT privacy, augmented reality |
| **IAA Mobility, Germany** | AVL, Valeo | • Massively distributed array of optical sensors;<br>• The fuel cell DC/DC power conversion performances |
| **IEEE European Test Symposium** | Cogninn | SW/HW solutions in the implementation of open RAN |
| **IEEE International Symposium for Design and Technology in Electronic Packaging, Romania** | Semikron-SK | • Implementation of packaging principles for power electronic package<br>• The influence of humidity and environment in the model performances |
| **EMC Europe** | Valeo | • Electromagnetic compatibility model for power electronics switching elements<br>• Inter component coupling and couplings with their close environment<br>• Standard method based on hybrid time and frequency domain to accelerate simulation of power electronics |
| **Intelligent Transport Systems European Congress** | AVL, Continental-FR, Vitesco | • Instrumentation and test systems for microelectronics automotive testing<br>• Software-defined vehicle: the processing unit as an enabler<br>• Wide bandgap benefits in the context of transportation solutions |
| **European Conference on Power Electronics and Applications** | AVL, EEMCO, FMC, Renault, Semikron-DE, Soitec, Valeo, Vitesco, ZF | • Switching cell performances using an advanced SiC power module in the context of a traction inverter<br>• The estimation and evaluation of wide bandgap based components reliability |
| **International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, Austria** | EEMCO | Crystal growth advanced processes applied to SiC manufacturing |
| **European Association for Cancer Research** | Menarini | Application of the project results to oncology |
| **European Solid-State Device Research Conference** | AT&S, Bizzcom, Continium, IFX-AT, R&S, Semikron-SK, Soitec, STM-FR, STM-IT, | • Holistic simulation approaches in IC substrate and PCB advanced packaging for better efficiency, performance and reliability |

| Conference Title, Location ([16]) | Participating undertakings | Main topics addressed (examples) |
|---|---|---|
| | STM-MT, X-FAB-FR | • Cutting edge-AI technologies and solutions offering for specific memristor-based neuromorphic applications<br>• Improved power electronic package: evaluation in the field of humidity model and performance<br>• Heterojunction Bipolar Transistor device based on SiGe technology |
| **Mobile World Congress, Barcelona** | Airbus AT&S, GF, IFX-DE, Nokia-FI, NXP-AT, NXP-NL | • Post-quantum cryptography applied to secure elements for mobile applications<br>• 6G product demonstrators applied to possible use-cases |
| **SIA Powertrain & Energy Congress, France** | FCM, IFX-DE, MEMC, mi2, Osram, Renault, Vitesco, X-FAB-DE | • Energy-Filter for ion implantation technology<br>• Advanced power electronics system and/or its best integration into next gen of e-drive system |
| **RADiation Effects on Components and Systems, Italy** | Teledyne | Components (i.e., data converters, processors) for advanced SiP in flip-chip organic |
| **Embedded Real Time Systems** | AVL, Codasip, Continental-FR, NXP-AT, NXP-RO | • The application of RISC-V based processing units<br>• Advances in embedded real-time system design, development<br>• HPC solutions applied in innovative automotive architectures |
| **SEMICON Europa** | AT&S, Bosch-DE, Continium, IFX-AT, NXP-NL, SGL, Soitec | • IC Substrates for HPC<br>• Packaging of CMOS image sensors and integration of readout electronics<br>• Requirements for inline inspection and metrology systems for advanced node semiconductor manufacturing |
| **Sensors Europe** | AT&S | The application of 5G to the industry |
| **International VDI Electronics In Vehicles Congress, Germany** | AVL, Continental-FR, GF, IFX-DE, KDPOF, Renault, UMS | • Validation systems for ADAS/AD sensors & ECU/DCU in automated vehicles<br>• Scalable Automotive E/E architecture |
| **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis** | IFX-AT, Osram, STM-FR, STM-IT, Sunlight, Valeo, Vitesco | • Wafer and panel-level interconnection technologies<br>• Power switch failure mechanisms and reliability |
| **International Conference on Advanced Semiconductor Devices and Microsystems, Slovakia** | ADI, AT&S, Continium, IFX-AT, Osram | • Novel packaging technologies, design / co design to achieve fine lines, high efficiency, optical integration, higher layer counts<br>• Advance high voltage bipolar and Diffused Metal Oxide semiconductors |
| **SPIE Photonics Europe** | Aledia, ASML, Bosch-DE, FCM, Osram, Trumpf Photonic, Vigo | • Findings on µLED development and InP Laser development<br>• Achievements in the development of the mid-infrared integrated photonics platform<br>• mid-infrared PIC-based devices and |

| Conference Title, Location ([16]) | Participating undertakings | Main topics addressed (examples) |
|---|---|---|
| | | systems for sensing applications<br>• Lithography, mask and patterning |
| **The Design and Verification Conference & Exhibition Europe, Germany** | IFX-DE, MEMC, NXP-AT, NXP-NL, X-FAB-DE | • RISC-V low-power and secure design<br>• Application of quality control for mixed technologies in semiconductor fabs<br>• The use of AI/ML applications in semiconductor fabrication<br>• Device simulation and verification applied to high-frequency components for 6G |
| **RISC-V Summit Europe** | Codasip, IRVI, NXP-RO, Openchip | • EDA tool extensions for RISC-V core design<br>• HPC RISC-V SW/HWsolutions |
| **Vision, Germany** | Teledyne | Integration of vision modules thanks to SiP |
| **Workshop of the German Society for Crystal Growth and Crystal Chemistry on Epitaxy of III-V Semiconductors, Germany** | EEMCO, Soitec | • Advanced crystal growth processes for III-V semiconductors<br>• Device performance and reliability on smart SiC |
| **Electronics displays conference, Germany** | Aledia | GaN microLED performances and components |
| **LETI innovation days, France** | Aledia | GaN microLED performances and components |
| **Electronica, Germany** | AT&S, Continium, Cologne Chip, IFX-AT, IFX-DE, NXP-NL, NXP-RO, Soitec, Teledyne, Valeo, X-FAB-FR | • Integrated power GaN innovation on 200mm wafer<br>• Advanced SiP in flip-chip organic<br>• SiC technology robustness in linear mode |

***Table 4: Events/conferences where at least one participating undertaking will participate***

#### 2.5.1.3. Dissemination and spillovers through the Union collaborative R&D&I ecosystem

(244) The participating undertakings commit to disseminate the IP non-protected results acquired in the framework of IPCEI ME/CT to the scientific community. In particular, the participating undertakings will collaborate with associated participants and with indirect partners (see sections 2.5.4 and 2.5.5).

(245) The participating undertakings will, in particular, finance and contribute to the creation or development of university chairs related to technologies developed under IPCEI ME/CT with a view to train future European scientists, experts, engineers, technicians and operators. The locations of the research organisations ("ROs") go beyond the Member States, thus providing genuine spillover effects to e.g., Belgium, Croatia, Hungary, Portugal and Sweden.

(246) It is expected that the following indicative list of ROs will benefit from the dissemination of the results of IPCEI ME/CT:

| Institution (example) | Participating undertakings | Scope of the Funding/Collaboration ([17]) | Member State |
|---|---|---|---|
| **Austrian Institute of Technology** | EEMCO, NXP- AT | Security concepts for RISC-V, sustainable components, AI-based methods for fully automated advanced equipment for SiC single crystal growth | Austria |
| **B-Com** | Airbus | Development of 5G applications, addition of broadcast capabilities to networks | France |
| **Brno University of Technology** | Codasip, Mycroft | Security algorithms, embedded AI modules | Czechia |
| **Chalmers University of Technology** | […], R&S | […], development of a next generation over-the-air measurement method and test platform | Sweden |
| **Delft University of Technology** | NXP-AT, NXP-NL | Novel concepts for energy-efficient battery management systems, mmW technology, antenna systems in highly integrated sub-terahertz ("subTHz") automotive radio front-ends | The Netherlands |
| **Eindhoven University of Technology** | Nearfield, NXP-AT, NXP-DE, NXP-NL, Vigo | Security concepts for post-quantum cryptography, mmW circuit concepts for subTHz radar radio front-ends | The Netherlands |
| **Fraunhofer Society** | AVL, Bosch-DE, Continium, EEMCO, Elmos, GF, Lynred, mi2, Nokia-DE, NXP-RO, Osram, R&S, SIAE, Semikron-DE, Soitec, UMS, X-FAB-DE | Installation support of an open-source foundry and research on epi-less substrates, drift-zone doping and superjunction devices, next generation radar platform software, piezoelectronic materials, antenna in package technology for subTHz, evaluation of new sensor integration routes | Germany |
| **Gheorghe Asachi Technical University of Iasi** | Continental-RO, NXP-RO | HW/SW co-design for domain specific accelerators, security longevity and vulnerability analysis, next generation sensors | Romania |
| **Gipsa-Lab** | Lynred | Sensor algorithms | France |
| **GREMI** | STM-FR | GaN,/ aluminium gallium nitride ("AIGaN") cryogenic atomic layer etching and deep buffer etching process | France |
| **IMT Mines Albi** | MEMC | Machine learning based tool for assisted tuning of epitaxial reactors | France |
| **Institute of Electrical Engineering, Slovak Academy of Sciences** | Bizzcom | Atomic layer deposition of memristors, crossbars and their characterisation | Slovakia |
| **Institut Mines** | STM-FR | SHIFT research project: Sustainable technologies enabling future telecom applications | France |
| **NaMLab** | FCM, GF | Hydride vapour phase epitaxy crystal growing processes | Germany |
| **Technical University Dreseden** | Ericson, R&S | 6G research and hardware development with a focus on antenna | Germany |

([17]) As general overview/examples presented. Individual projects include a detailed description for each participating undertaking.

| | | | |
|---|---|---|---|
| | | in package technology for subTHz frequencies, radio sensing capabilities in 6G radio systems | |
| **Technical University Graz** | AVL, NXP-AT | Sensor fusion, perception technologies, AI training, new sensor concepts and production processes, security concepts for RISC-V, battery management concepts | Austria |
| **Technical University of Denmark** | MEMC | Modelling and design of a quantum-driven IoT architecture, machine and deep learning applications for improving quality and yield | Denmark |
| **Technical University of Kosice** | Semikron-SK, Tachyum | Intermetallic compound formation, evolution and stability in joints based on new types of alloys, universal processor research | Slovakia |
| **Technical University Vienna** | IFX-AT, Nokia-DE | Massive-MIMO antennas concepts for 5G/6G radio technology, process simulation for virtual technology development | Austria |
| **Tyndall National Institute** | ADI, Osram, Vigo, VLC, X-FAB-DE | Heterointegration of photonic and electronic components for sensor fusion, Si manufacturing and charaterisation | Ireland |
| **UCLouvain** | NXP-AT, Soitec | Security concepts for post-quantum cryptography, testing of wafers for high frequency domains | Belgium |
| **Università di Bologna** | Openchip | Power management, HW/SW IP | Italy |
| **Universitat Politecnica de Valencia** | FCM | Nanolaser research for photonic chip applications, | Spain |
| **University Gustave Eiffel** | Lynred, X-FAB-FR | Infrared sensor specifications, thermal management of heterogeneous integration of GaN on Si | France |
| **University of Extremadura** | IRVI | Viability of the integration of power devices in system-on-a-chip (“SoC”) | Spain |
| **University of Malta** | STM-MT | Smart sensor nodes for process equipment real-time monitoring, analysis of robotised factory for production optimization | Malta |
| **University of Tampere** | Nokia | SoC design capabilities | Finland |
| **University of Thessaly** | Sunlight | BMS IC products | Greece |
| **University of Twente** | ASML, Menarini | AI algorithms for processing of sensor data, machine learning interference technology, holistic lithography innovations | The Netherlands |
| **Uppsala University** | Codasip | Specification and development of accelerators | Sweden |
| **Zilina University** | Bizzcom, Semikron-SK | Fuzzy logic function HW/SW design, development of new production processes and packaging and encapsulation techniques | Slovakia |

***Table 5: Non-exhaustive network of RO, benefitting from spillover effects with participating undertakings***

#### 2.5.1.4. Dissemination and spillovers through publications in scientific journals

(247) The participating undertakings will, over the course of IPCEI ME/CT, disseminate their research results in various scientific peer reviewed journals either Europe-wide and/or globally. The following table displays some indicative examples:

| Journal Title | Scope of Journal |
|---|---|
| **Advanced Materials** | Material sciences, interdisciplinary focus on chemistry and physics of functional materials. |
| **ACS Nano** | Nanoscience and nanotechnology research on synthesis, assembly, characterization, theory and simulation of nanostructures, nanobiotechnology, nanofabrication, methods and tools, and self- and directed-assembly. |
| **Advances in Materials Science and Engineering** | Materials science and engineering, synthesis and properties of materials, applications in engineering. |
| **Applied Materials & Interfaces** | Biological and medical applications of materials and interfaces; energy, environmental and catalysis applications; functional inorganic materials and devices; organic electronic devices; functional nanostructured materials, applications of polymer, composite and coating materials; surfaces, interfaces and applications. |
| **Biomedical Optics Express** | Optics, photonics and optical imaging in biomedicine. |
| **ChemElectroChem** | Electrochemistry research, including energy applications, interfaces, photo- and bioelectrochemistry. |
| **Chip** | Integrated chips research on rapid development and potential application of new-generation information technologies. |
| **Computational Materials Science** | Application of modern computational methods alone or in conjunction with experimental techniques to discover new materials and investigate existing inorganic, organic and hybrid materials. |
| **Enterprise AI** | Machine/deep learning, advanced modelling/simulation, high-performance data analytics and technologies, including high-performance data centres, cloud computing, high-performance storage, AI Si and AI frameworks. |
| **EUMA International Journal on Microwave and Wireless Technologies** | Applied electromagnetic field theory, components, analogue and mixed-signal circuits, systems, optical-microwave interactions, electromagnetic compatibility, industrial applications, biological effects and medical applications. |
| **Frontiers in Oncology** | Cancer epidemiology, molecular pathways, diagnosis and imaging, personalised therapeutics, and novel treatment and management strategies. |
| **IEEE Journal of Microelectromechanical Systems** | Microelectronic devices, IC-compatible fabrication techniques, measurement of microphenomena, new materials and designs, microactuators, microrobots, microbatteries, bearings, wear, reliability, electrical interconnectors, microtelemanipulation and standards appropriate to MEMS. |
| **IEEE Transactions on Transportation Electrification** | Components, grid-interfaced technologies, standards, sub-systems and systems related to power and energy conversion, propulsion and actuation for all types of electrified vehicles, airplanes and ships. |
| **Journal of Applied Crystallography** | Methods and use in identifying structural and diffusion-controlled phase transformations, structure-property relationships, structural changes of defects, interfaces and surfaces. |
| **Journal of Astronomical Telescopes, Instruments, and Systems** | Development, testing and application of telescopes, instrumentation, techniques and systems for ground- and space-based astronomy. |
| **Journal of Network and Systems** | Research on communication and computing aspects of modern network |

| | |
|---|---|
| **Management** | and service technologies, including 5G, IoT, SW-defined networks, high-precision networks, security, VR/AR services, network function virtualization, edge-computing, network slicing, in-band network telemetry, DL and big data analysis. |
| **Journal of Vacuum Science and Technology** | Surface science, electronic materials and processing, fusion technology, plasma technology, thin films, vacuum metallurgy and vacuum technology. |
| **MDPO Computers** | Computer and network architecture and computer-human interaction. |
| **Nature Photonics** | Research into fundamental properties of lights and interactions with matter, design of optoelectronic devices and emerging photonic application. |
| **Nuclear Instruments and Methods in Physics Research** | Design, development and performance of scientific instruments, including complex detector systems and large-scale facilities, which utiliSe or study ionizing radiation. |
| **Optical Engineering** | Imaging components, systems and processing; optical instrumentation, techniques and measurement; optical design and engineering; lasers, fiber optics and communications; optical materials, photonic devices and sensors. |
| **Precision Engineering – Journal of the International Societies for Precision Engineering and Nanotechnology** | High accuracy engineering, metrology and manufacturing of high precision, machines, instruments and components of various sizes from nanotechnology to large-scale systems. |
| **Proceedings of the ACM International Conference on Supercomputing** | Architecture of high-performance computers and computation including, power-aware, parallel input/output, grid-based, web-based, continuous monitoring, self-healing, fault-tolerant, embedded. Productivity research including benchmarks, performance evaluation, specialized languages, program development tools. Systems research, including compilers, operating systems, schedulers, runtime optimization. Applications research, including numeric and non-numeric, scientific, biological, industrial, massive sensory processing. |
| **Sensors and Actuators A: Physical** | Research on solid-state devices for transducing physical signals: Fundamentals, materials, processing, optoelectronic sensors, mechanical sensor, thermal sensors, magnetic sensors, micromechanics, interface electronics, sensor systems and applications. |
| **Solar RLL** | Solar energy conversion research on photovoltaics and solar cells; development, characterization and optimization of materials and devices; photovoltaic modules and systems; installation and deployment; photocatalysis, solar fuels, photothermal and photoelectrochemical solar energy conversion; energy distribution and grid issues. |
| **Springer Journal of Cryptographic Engineering** | Architectures, algorithms, techniques, tools, implementations and applications in cryptographic engineering, including cryptographic hardware, embedded systems, side-channel attacks and countermeasures and embedded security. |
| **Thin Solid Films** | Thin film synthesis and control of growth; surfaces and interfaces; solar energy conversion; catalysis; batteries and other electrochemical devices; metallurgical, protective and hard coatings; electronics, optics and optoelectronics; magnetics and magneto-optics; superconductivity. |
| **Transactions of Cryptographic Hardware and Embedded Systems** | Design and analysis of cryptographic hardware and software implementations, including cryptographic implementations, attacks against implementations and countermeasures, cryptographic tools and methodologies, cryptographic implementation issues and applications. |

2. ***Table 6: Representation of scientific journals in IPCEI ME/CT***

#### 2.5.1.5. Dissemination and spillovers through training events

(248) The participating undertakings have committed to organise educational academic dissemination through dedicated training of professionals and researchers. The envisaged activities follow up on the R&D of new products and designs, production processes, materials and technologies under IPCEI ME/CT and aim to strengthen the skills of those involved and maintain competitiveness in the microelectronics and

communication technologies markets. The training activities will cover a broad range of formats, such as regular series of lectures, technical trainings, VR programmes, academies and summer schools, remote online modules/e-learning platforms, hackathons, exchange programmes and internships and will cover various issues, such as: use cases for RAN presentation on private networks, security, decarbonisation, sustainable mobility, advantages of GaAs technology for power electronics, centralised electrical and electronic architecture, circuit design with ADC/DAC, SiC frontend and backend processes, inertial MEMS in automotive and industrial applications, application of AI/ML, sensing systems for early-stage detection of cancer biomarkers, photonics, etc. Each of the training activities that a participating undertaking has committed to provide is set out in more detail in its respective individual project portfolio, where some additional examples are provided in section 2.5.3.

*2.5.2. Dissemination and spillover of results that is protected by IP rights*

(249) The participating undertakings have committed to disseminate the IP-protected results achieved through their individual projects under IPCEI ME/CT. This dissemination will be carried out in different ways. However, all participating undertakings will disseminate the IP-protected results of their individual projects under IPCEI ME/CT on fair, reasonable, and non-discriminatory terms ("FRAND").

(250) Indicatively, some concrete examples of committed dissemination activities are presented in the following:

(251) Aledia will use the Minalogic cluster to disseminate information about licensing opportunities for RO and SME. The undertaking will offer licenses connected to its R&D on growth epitaxy GaN on Si and smart pixels for display applications. Licenses will be offered to undertakings working on power GaN, radio-frequency applications, display manufacturing and hybrid bonding for imaging technologies.

(252) ADI explains that it will license IP-protected technologies related to the manufacturing of advanced precision analog Si on FRAND terms and will provide additional information on intended application and problem-solving support under confidentiality agreements. The undertaking cooperates with RO and enables various forms of licensing for further research and commercial exploitation.

(253) ADVA will generate IP-protected results related to Si photonics, control electronics, high-speed electronics, laser and digital signal processor ("DSP"). Results will be licensed under FRAND conditions to European entities. The technologies will be showcased at industry events and conferences to disseminate R&D results to potential partners.

(254) Airbus intends to develop a set of innovative 5G capabilities for sovereign mission-critical communication solutions, […]. Airbus commits to grant non-exclusive and non-transferable licenses to third parties through an open and transparent selection process.

(255) AVL will generate IP-protected results related to advanced drive assistance systems ("ADAS")/automated driving ("AD") sensors and electronic control unit ("ECU") / digital control unit ("DCU") in automated vehicles, technologies for validation systems of safe and secure chips in connected vehicles, and power chips for power electronic testing and validation tools. AVL commits to providing licenses on

FRAND terms on a non-exclusive, and either royalty-bearing or royalty-free basis, to European ROs and SMEs, depending on the type of the cooperation.

(256) BLK will create patents related to the technology required for the fabrication of graphene- and Si-based photonic devices. The main strategy to advertise the novel technology is contacting peers, customers, and interested persons at trade fairs and online presentations. Moreover, cooperation with universities, a newsletter and social media will be used to spread the knowledge about the technology. BLK is also a member of the European Photonics Industry Consortium ("EPIC") and will actively use the services from EPIC to connect to European customers and SMEs.

(257) Cogninn will submit five patents at the European Patents Office for the vORAN technologies developed within the project. The main elements of the patent submission will relate to the O-DU and RIC components, as well as the virtualized elements of vORAN. Cogninn will fully own the patents and provide licensing possibilities for relevant IPs to interested parties under non-exclusive FRAND terms.

(258) Continental-FR will develop an innovative electronic architecture for automotive systems using high-performances central and ZCU based on RISC-V. Continental-FR commits to license IP protected results, with priority given to European entities, through non-exclusive licenses negotiated under FRAND conditions.

(259) Continium will provide licenses for its continuous-time sigma-delta ADC product design via dedicated Si IP internet portals for automotive radar and liDAR, military radar, wireless base stations chipsets and other wireless products.

(260) EEMCO will grant licences covering mainly the process know-how regarding crystal growth furnaces. Additionally, specific licences might allow to test and potentially use a novel SiC-powder. Partners will be able to gain optimum alignment of SiC material properties along the value chain from puck fabrication to electronic devices. For specific strategic business and R&D - partners EEMCO will also share process- and product data for deep analysis to implement advanced process control loops from crystal to device making.

(261) FCM will generate IP-protected results on GaAs-, InP- and GaN crystal growth, wafer manufacturing and conditioning and the associated metrology. FCM commits to license based on FRAND conditions except to direct competitors. FCM will announce its results and the possibility of licensing the protected results on the company's website and will advertise this announcement to potential parties at conferences and meetings with partners inside and outside the IPCEI.

(262) GF commits to license its FD-SOI technologies developed within IPCEI ME/CT at FRAND terms to all interested parties in the European value chain, including partners, customers, SMEs and ROs, thereby promoting the dissemination of key technological advancements.

(263) IFX-AT will disseminate information about the possibility of obtaining IP-protected results on FRAND related to power semiconductor devices. It will communicate the IP-protected results through newsletters, websites and specific IP-related workshops.

(264) Lynred will publicise IP-protected results and opportunities for exploitation via the Minalogic cluster, presentations and workshops. The IP will be generated from research on infrared sensors, uncooled micro-bolometers and cryo-cooling systems.

(265) MEMC will generate IP protected knowledge about Si wafer production and modification, characterisation techniques, and metrology industry standards. The undertaking will license patents to all interested European entities. In addition to that, R&D results will be presented at events and conferences to promote licensing opportunities.

(266) Menarini will conduct research on the detection and classification of rare cells in microfluidic channels, AI for automated cell classification and sorting of pure, viable single rare cells from heterogeneous samples. IP-protected results will be licenses on FRAND and made available to clinical studies and research-oriented investigations.

(267) mi2 will grant licenses related to energy-filter technology, accelerator and ion source, implantation setup, chip and substrate application, and application simulation SW on FRAND terms.

(268) Nokia-FI will generate IP protected results related to Advanced 5G, 6G and edge-AI electronics. The results will be licensed under FRAND conditions to […] entities. The developed technologies will be also showcased in industry events.

(269) NXP-DE commits to establish multiple patents […] data converters that are used for base stations and digital signal processing. These patents, which are technically essential for the implementation of applicable standards, will be licensed on a non-exclusive basis to interested European entities on FRAND terms.

(270) NXP-RO has identified a list of areas where it will generate exploitable foreground IP including: algorithms for radar in advanced interference mitigation processing and neural net radar perception; optimisation of AI/ML models for resource constrained devices; 6G algorithms; isolation configuration and verification tools. Information on the IP-protected technologies will be disseminated via academic journals and conferences.

(271) Osram commits to grant access rights with respect to the foreground IP generated by its project, to other IPCEI ME/CT participating undertakings and to interested third parties in particular SMEs and start-ups, through licensing on FRAND terms.

(272) R&S will license IP-protected results covering instrument concepts, monolithic microwave IC ("MMIC") designs and circuit applications of the GAN technology on non-exclusive terms to European SMEs and ROs. […].

(273) Semikron-SK will generate IP-protected results related to power electronic package technologies, encapsulation technologies and contacting technologies. Results will be licensed under FRAND conditions to European entities. These technologies will also be showcased at industry events and conferences.

(274) Soitec will generate IP in the areas process technology, metrology and new materials for engineered substrates. European SMEs and ROs will be offered licenses on FRAND terms.

(275) Thermo Fisher will generate IP-protected results mainly in the area of improved Transmission Electron Microscopy workflows. Access to protected IP will be granted to any European entity under FRAND conditions, provided any commercial use takes place outside the field of business of Thermo Fisher and its affiliates. IP-

protected results will be disseminated via symposia and conferences targeting the semiconductor equipment and the wider high-tech equipment ecosystems.

(276) Valeo will grant licenses for IP protected results related to power electronics for the automotive and mobility sectors to European entities on FRAND terms.

(277) Vigo will generate new IP-protected results through R&D activities on mid-infrared light sources and detectors, passive photonic IC, integration, assembly and packaging, and mass testing techniques. Access to appropriate non-exclusive licenses will be offered to European entities under FRAND conditions. The developed technologies will also be demonstrated at industry trade events, workshops, and conferences.

(278) Vitesco will develop high voltage power electronic products adapted to wide bandgap technologies (SiC and GaN). Vitesco commits to grant non-exclusive license under FRAND condition regarding the foreground IP protected results.

(279) Wacker will grant access to IP protected innovations on FRAND terms to other European entities. The patents should relate to […] crushing, […] sorter and etched polysilicon and the optimisation of the integrated process between these elements.

(280) Zeiss will generate new IP-protected results on extreme-ultra-violet lithography optics and photomask equipment. Licenses will be granted on FRAND terms to European entities outside of the field of business of Zeiss and its affiliates.

(281) ZF commits to license on FRAND terms the power module IP interested parties in the European microelectronics and communication technologies value chain, including partners, customers, SMEs and ROs, thereby promoting the dissemination of key technological advancements and accelerating the scaling of cost-effective SiC devices.

### *2.5.3. Dissemination and spillover of results in FID*

(282) The participating undertakings that will carry out FID activities will use several ways for disseminating results generated during that phase. The Member States have provided information showing that the FID activities will lead to spillover effects in downstream markets among the participating undertakings but also beyond them, involving indirect partners and the society in general. A close collaboration with ROs and SMEs is inevitable to scale-up technologies from laboratory to industrial scale. Moreover, providing access to pilot lines for, among others, testing and validation of products and services to a wide range of industrial entities is necessary to spread the results during FID. Standardisation activities will also serve as a means to support exploitation and dissemination.

(283) In particular, many participating undertakings have committed themselves to provide design kits, often free of charge, to IPCEI ME/CT indirect partners, SMEs, start-ups, universities and ROs (see recital (315)). Design kits are PCB equipped with semiconductor devices and further electrical components. They enable engineers to become familiar with the technology, prototype applications and test performance.

(284) Moreover, multi-project wafers (“MPW”) enable close collaboration between different parties (i.e., participating undertakings, associated participants, indirect partners and other interested parties). The parties involved can share mask and

microelectronics wafer fabrication costs between several designs or projects. In a MPW different chip designs are aggregated on a wafer. Novel mask making and exposure systems in photolithography enable this type of manufacturing. Multiple participating undertakings have committed themselves to provide MPW opportunities.

(285) Some examples of dissemination activities in FID are provided in the following.

(286) Aledia commits to collaborate with research labs and SMEs in order to share know-how related to the implementation of epitaxy equipment. Aledia will organize pilot-line visits and events with laboratories and SMEs. It will organise these activities with the support of industry alliances and clusters, in order to reach a large scope of potential interested parties.

(287) ASML will make high-NA EUV technology available in a pilot line at the Interuniversity Microelectronics Centre ("IMEC"). In collaboration with IMEC, manufacturing expertise will be established and shared with partners. The lithographic infrastructure will be open to all parties in the microelectronics and communication technologies value chain to enable their development of next generation process technology and equipment.

(288) AT&S will grant universities, ROs and SMEs access to the FID site and provide hands-on training for its newly developed technologies. These activities will include the organisation of a large-scale forum, a prototyping workshop as well as guest visits. In addition, AT&S will take part in a bi-annual event where the FID site and the technology will be opened to the general public.

(289) Bizzcom will grant various stakeholders, including SMEs and ROs, access to their technology and production facility. This will include guided visits, the provision of testing kits and chips and the renting out of access for other undertakings to test their own inventions. Additionally, collaboration with original equipment manufacturers ("OEM") and suppliers will lead to knowledge-sharing with the automotive sector. The undertaking will be involved in MPW design activities and testing.

(290) BLK commits to provide process design kits to interested parties for the design of their own photonic products in a fabless-mode. Moreover, for the dissemination of results during the FID phase, the undertaking will collaborate with industry alliances, host public workshops and participate in conferences and trade fairs.

(291) Bosch-DE will issue test kits to ROs and universities with requirement to provide reports on the application. The kits will be equipped with advanced sensors and power chips. Moreover, the undertaking will provide foundry services for testing and optimising purposes of new products and workshops on coating, metrology and laser technologies, equipment handling, process automation and cleanroom infrastructure based on its experiences in the FID phase.

(292) Cologne Chip will cooperate with open SW providers and other vendors to disseminate the newly developed chips. The undertaking will provide evaluation boards to potential customers, universities and ROs to gather feedback and support the development of multiple applications in the telecommunication, automotive, mechanical engineering, healthcare and aviation sectors. Cologne Chip will reach out to SMEs through a targeted ad campaign, technical press and a network of distributors.

(293) Continium will provide prototypes of broadband ADCs for wireless applications to other entities for their system evaluation. To support the dissemination, Continium will host a wireless conference and establish an openRAN community.

(294) EEMCO will provide access to next generation material and new technologies to partners, SMEs and ROs. This will include the exchange of datasets for the development of models and simulations of single crystal growth. In addition, EEMCO will provide a platform for its scientific partners, where the results of simulations can be tested and validated. Furthermore, collaboration during the FID phase will generate dissemination spillovers to OEMs, suppliers, manufacturers and ROs.

(295) FCM develops large diameter substrates. The production requires special equipment and processes, which need to be modified according to the specifications of the target application. The modifications will be done in collaboration with partners to adjust the measurement technology and manufacturing equipment. Feedback loops for characterization and testing will improve the results. FCM will also engage in standardisation activities and incorporate the results of its projects into standards, where applicable.

(296) FMC will design product macros that are specified in close alignment with SMEs that desire to utilise FMC's memory technology for AI chip designs and design companies providing memory macro specifications. The exchanges will be used to test new chip products.

(297) GF commits to provide MPW to universities and ROs (i.e., test dies to be measured at universities and ROs and receive feedback on specific behaviours). It will furthermore offer SMEs and smaller design undertakings, access to GF's manufacturing lines, as well as supply them with product/SW design kits, thereby enabling them to test their products, while at the same time stimulating the diffusion of innovation developed in IPCEI ME/CT.

(298) IFX-AT commits to grant partners, universities and SMEs access to test their new technologies and products before they become commercially available. They will be able to provide feedback for further improvement and shorten the time-to-market for their own related products. To do so, the undertaking will give out application-oriented HW/SW kits to increase the understanding of power electronics and enable experimental developments and fast prototyping of new applications.

(299) IFX-DE commits to provide to SMEs and ROs a MPW run comprising of 250 wafers, enabling them to get access to IFX-DE's latest technology and test their projects. In particular, this is planned to take place within the context of precompetitive research projects or bilateral collaborations, whereby IFX-DE will provide the collaboration partners a circuit design kit to facilitate the design of their own dedicated circuits.

(300) Lynred will use the FID phase to increase and stabilise yields of the sensor production to reduce costs. Based on the collaboration with initial customers key parameters for efficiency can be improved. This includes granting access to testing platforms and the distribution of platform and SW development kits for the joint development of bolometer sensors and advanced detection circuit technologies.

(301) Menarini will offer facility visits and trainings for interested parties as well as technical support for medical and lab personnel. During the FID phase, partners will gain early access to instruments and cartridges and receive free instrument loans for validation of the single cell sorting technology in clinical research and practice. The undertaking will receive feedback on usability, validity and robustness from the partners.

(302) Nearfield will provide ROs and SMEs with access at a zero-rate to a pilot line to test samples on its systems to assess new applications and evaluate their performance.

(303) NXP-AT will contribute to a concerted approach for technological dissemination through standardisation of RISC-V, postquantum cryptography and including UWB implementations in international standard setting bodies. It will train engineers to achieve interoperability and extend the product use to multiple value chains, including the combination of UWB with radar and LiDAR, as well as the combination of components based on different architectures. Moreover, NXP-AT will collaborate with other entities for performance and vulnerability testing.

(304) NXP-DE will provide access to leading-edge technologies in the form of test vehicles to ROs and universities, enabling them to gain first application experiences and improve their technological acceptance. NXP-DE will furthermore supply downstream value chain partners with new developed technologies and test concepts (e.g., SW development and evaluation kits), thereby facilitating system integration and the generation of new use cases and business ideas.

(305) Orange will work with the O-RAN ecosystem, network management vendors, automotive and industry partners during the FID phase. The undertaking will offer access to its testing platforms, make documentation and source code of the stack available as open-source and communicate the results of its testing activities.

(306) SGL will use the FID phase to construct an advanced coating centre […]. The undertaking will share process know-how with SMEs and ROs on […] coating and share the results with the business and academic communities, including through trial runs, lab visits and joint research.

(307) STM-FR, STM-IT and STM-MT will host start-ups at its sites to provide them with technological and product support using FID outputs. The undertakings will provide start-ups, ROs and SMEs with MPW services, including hands-on training, and provide design kits to test and develop their products.

(308) Vigo will organise trainings and workshops on mid-infrared photonic integration technology. It will also offer SMEs and ROs opportunities to participate in MPW runs and will provide PDKs for all MPW participants. Moreover, Vigo will develop technological standards for the designing, manufacturing and testing of the HyperPIC platform.

(309) Vitesco will share the results of its FID activities in working groups with partners from the automotive sectors. This will concern information on the reliability of SiC and GaN power components and systems, standardization requirements, and electronics lifecycle and carbon footprint analysis. Moreover, it will offer the possibility for ROs to use prototypes to enable their own product development.

(310) X-FAB-FR will enable SMEs and ROs to develop and test prototypes at its foundry and have free access to design kits. Reengineering of the technology will be performed to configure it to the specific end user requirements. This process will be supported through facility visits and workshops to disseminate information to stakeholders.

(311) Zeiss will produce first tool prototypes during FID and will integrate them into the manufacturing processes to produce advanced IC products. This will be done in collaboration with project partners and universities. Scanner manufacturer will gain access to key optics performance results to evaluate the results of the tool application. The learning process will allow the partners to gain insights into the performance of optical tools over their lifecycle and the impact of the physical and chemical processes on the components.

*2.5.4. Dissemination and spillover of results to the associated participants*

(312) The participating undertakings will collaborate with all of the 46 associated participants to achieve the objectives of their individual projects, as well as those of the four WS of IPCEI ME/CT. As a result of these collaborations, the benefits of IPCEI ME/CT are not limited to the participating undertakings but are extended to other undertakings and ROs that participated initially in the design of IPCEI ME/CT and will contribute to it with their own individual project (see recital (47)). The following examples are illustrative of the various collaborations and objectives pursued:

- The collaboration between ADI and Applied Materials GmbH (Germany) will enable the development of non-contact metrology on packaging solutions for sensors in the healthcare sector. ADI will develop the integrated sensor systems, while Applied Materials GmbH will work on the characterisation of prototypes using non-contact metrology system and will support the research about advanced packaging techniques;

- AT&S and […] have agreed to collaborate with the purpose of conducting research and developing AFM for future 6G radios. AT&S will design, simulate and manufacture a substrate for an integrated front-end MCM for future AAS radios in the frequency range of 6-15 GHz, while […] will provide smart substrate, cooling technologies and a heterogeneous integration assembly;

- IFX-DE and Derivados del Flúor, S.A.U. (Spain) will jointly work to improve wet-chemical processes and reduction of impurities for the fabrication of chips based on new smaller nodes. Derivados del Flúor, S.A.U. will develop new production processes, test new materials for purification and develop new analytical methods to measure impurities, while IFX-DE will test the resulting products at its production lines and analyse performance and compliance with requirements of new smaller node dimension chips;

- Trumpf Photonic and Fondazione Bruno Kessler (Italy) have agreed to collaborate with the purpose of developing vertical cavity surface emitting lasers integrated into photonic platforms with the aim of building high performing communication systems. Trumpf Photonic will investigate whether SiP platforms could use the said lasers instead of InP lasers and whether this

substitution would bring any benefit, while Fondazione Bruno Kessler will use Trumpf Photonic's lasers in its Si integrated photonics sensing devices;

- The collaboration between Airbus and Akronic P.C. (Greece) aims to enable the development of advanced antenna solutions, […]. Airbus will develop different satellite and terrestrial 5G solutions, while Akronic P.C. will develop 5G beamforming antennas adapted to Airbus' solutions;

- X-Fab-FR and Soitec Belgium N.V. (Belgium) have agreed to collaborate with the purpose of enhancing research and increasing future supply of novel III-V dedicated materials. Driven by technology requirements to serve advanced communication systems, X-FAB-FR and Soitec Belgium N.V. will jointly work to create solutions that include GaN for 5G/6G applications;

- Nearfield and Nanometrisis (Greece) will jointly work to […] and optimise the diagnostic value of the information generated by 3DFD system in metrology and inspection applications by applying advanced signal processing and AI/ML methods. NFI will develop the 3DFD inspection and metrology system, while Nanometrisis will develop and apply AI/ML techniques and mathematical algorithms; and

- Continium and iPronics (Spain) have agreed to collaborate with the purpose of developing CMOS/SOI compatible amplifiers and data converters. iPronics will enhance accuracy and speed control of the monitoring and driving units that are key elements of their programmable photonic chips, while Continum will develop CMOS/SOI compatible amplifiers and data converters to monitor and control the iPronics programmable photonics system.

(313) Furthermore, according to the information provided by the Member States the associated participants are committed to the generation of spillover activities, under the responsibility of the relevant Member States, with the aim of ensuring wider relevance and application to the economy or society in the Union.

*2.5.5. Dissemination and spillover of results to other indirect partners and to other sectors*

(314) The participating undertakings have committed to disseminate knowledge and results arising from their individual projects with other undertakings, organisations and sectors outside IPCEI ME/CT, through the participating undertakings' participation in numerous collaborations with approximately 600 indirect partners, as shown in Table 5 under recital (246) and further supplemented below in recitals (317) to (320).

(315) The indirect partners are undertakings or organisations that have not submitted an individual project within IPCEI ME/CT. Nevertheless, they hold collaboration agreements with one or more participating undertakings of IPCEI ME/CT and they can therefore benefit from the various dissemination activities (e.g., wider infrastructure access, knowledge dissemination of R&D&I and FID results or open access to laboratory facilities, etc.).

(316) The participating undertakings commit to collaborate with several undertakings and ROs (see Table 5) from the same or different Member State inside or outside IPCEI ME/CT.

(317) In WS-SENSE, the participating undertakings will collaborate with 201 indirect partners. The Commission refers to the following collaborations as examples: Lynred (France) will collaborate with Fraunhofer (Germany) to define and evaluate new sensor integration routes; MEMC (Italy) will collaborate with CNR ISSMC Faenza (Italy) on Si wafer waste valorisation and examine the feasibility of waste reuse in civil construction; Osram (Germany) will collaborate with Picosun Oy (Finland) on the process and tool development for thin film layering to improve chip processing and package technologies; NXP-NL (the Netherlands) will collaborate with TuskIC (Belgium) on radio frequency circuit designs for automotive radar front-ends; NXP-RO (Romania) will collaborate with BEIA Consult International (Romania) on the SWe design for next generation radar, 6G and automotive platforms.

(318) In WS-THINK, the participating undertakings will collaborate with 234 indirect partners. For example, AT&S (Austria) will collaborate with SiPearl (France) to jointly design IC substrates for HPC; GF (Germany) will collaborate with […] to develop components for ultra-low-power communication technologies; Codasip (Czechia) will collaborate with the Institute of Communication and Computer Systems (Greece) on the design of metwor-based communications systems; and, Tachyum (Slovakia) will collaborate with the Technical University Prague (Czechia) on the development of a universal processor combining CPU, GPU and TPU.

(319) In WS-ACT, the participating undertakings will collaborate with 160 indirect partners. For example, AVL (Austria) will collaborate with Eos GmbH (Germany) to utilize innovative industrial additive manufacturing solutions for advanced testing tools of energy-efficient power electronics; IFX-DE (Germany) will collaborate with ASM (the Netherlands) on advanced process equipment for frontend manufacturing; MEMC (Italy) will collaborate with Semilab (Hungary) on advanced characterization methods to improve the lifetime performance of Si wafers; Semikron-SK (Slovakia) will collaborate with Pfarr (Germany) to develop and produce new solder materials and solder alloys; mi2 (Germany) will collaborate with […] on the adaptation of a cyclotron accelerator for SiC doping; STM-MT (Malta) will collaborate with the University of Malta (Malta) on process analysis, real-time monitoring of process equipment and packaging environment as well as the evaluation of the robotised factory for the optimization of productivity, safety, cycle time and cost.

(320) In WS-COMMUNICATE, the participating undertakings will collaborate with 296 indirect partners. For example, Ericsson (Germany) will collaborate with Corebone (Sweden) to produce high-performance materials for antenna radomes; Nokia-DE (Germany) will collaborate with the City of Ulm (Germany) to deploy public safety and smart city applications; SIAE (Italy) will collaborate with […] (France) on the design of a digital baseband processor for next generation wireless transport equipment; Continium (Slovakia) will collaborate with Rectangle (Poland) on the development and evaluation of boards for wireless receivers; ZF (Germany) will collaborate with Centrotherm (Germany) to sustainable improve SiC production capacity through the implementation of emission abatement technology.

(321) Furthermore, IPCEI ME/CT will generate spillover effects to other industries. Semiconductors are expected to be widely and urgently needed by many industries, including those developing communications systems, IoT devices and advanced technological products and solutions. Thus, the impact of developing new semiconductor technologies, materials, SW, production processes and manufacturing

equipment will be significant, allowing to increase connectivity, manufacturing efficiency and computer performance.

(322) The SW, manufacturing equipment, semiconductor components and semiconductors developed and produced by the various projects in the different WS are expected to be used by off-takers in multiple downstream sectors, including environment, agriculture, energy, automotive, health and space. For example, environmental monitoring can be improved through new sensors to track emissions and pollutions, fires and water fluxes (e.g., Mycroft's planned sensors and LiDAR can be used as ultra-low-power and highly sensitive sensors to monitor the content of pollutants in the atmosphere, to detect typical GHG at low quantities, and to monitor forest vegetation and water quality); undertakings in the agriculture sector can use new sensors for plant monitoring, optimised water management and optimised dispensing of fertilizer (e.g., Vigo plans to develop photonics technology, which will have key applications in the agricultural and food sector, allowing for the monitoring of crop condition, energy and water resource management, as well as the automation of agricultural operations); the energy sector will benefit from improved power conversion technologies (e.g., Valeo will introduce new power conversion technologies leading to innovative solutions for better energy management and performance of EV); transport firms can improve traffic management and command systems (e.g. SIAE plans to develop industrial wireless radio equipment and aggregate several mmW bands for enhanced traffic management); healthcare providers will be able to create new wearable health monitoring devices, bio-based sensors and bio-compatible components (e.g., STM-FR plans to support the development of HW/SW that allows the use of edge-AI capabilities with many types of sensors for multiple medical applications, notably diabetes care, patient monitoring at hospital, connected intelligent bandages, post-surgery monitoring etc.); new technologies and specialised sensors are planned to be developed for dedicated aerospace applications (e.g., Lynred's project will focus in the designing and manufacturing of infrared sensors for aerospace markets).

## 2.6. Description of the aid measures

### *2.6.1. Total eligible costs in IPCEI ME/CT*

(323) The notifying Member States indicate that the activities performed in the framework of IPCEI ME/CT qualify as R&D&I and FID in the meaning of points 22 to 24 of the IPCEI Communication.

(324) On the basis of the information contained in the individual project portfolios, and as summarised in section 2.4.1, the Member States submit that the nature and scope of the R&D&I projects falling within each of the WS covered by IPCEI ME/CT are such that those projects are of a major innovative nature or constitute an important added value in terms of R&D&I in the light of the state-of-the-art in the microelectronics and communication technologies sector. Furthermore, the Member States submit that this information also demonstrates that the FID projects will allow for the development of new products or services with high R&D&I content or the deployment of a fundamentally innovative production processes, going beyond mere upgrades without an innovative dimension of existing facilities or the development of newer versions of existing products. Moreover, according to the Member States, aid granted under IPCEI ME/CT is limited to R&D&I and FID projects and does not

cover commercial sales nor does it extend to the mass production phase of any of the products, services or processes resulting from the individual projects.

(325) The notifying Member States also submit that the total IPCEI ME/CT eligible costs ([18]) are approximately EUR 18.6 billion.

*2.6.2. Aid amounts per participating undertaking and per Member State*

(326) The Member States have submitted the amounts of State aid under the measures that they plan to provide to the participating undertakings, together with the individual eligible costs and funding gaps.

(327) According to point 33 of the IPCEI Communication, the maximum permitted aid level is determined with regard to the identified funding gap in relation to the eligible costs. The amounts of State aid are capped in nominal terms by the eligible costs, which are also presented in nominal terms. If the eligible costs are lower than the funding gap (in discounted net present value ("NPV") terms), then the eligible costs determine the maximum permitted aid level. If, however, the eligible costs are higher than the funding gap, then it is the funding gap that determines the maximum permitted aid level. Member States may choose to disburse State aid in several instalments over a certain period of time, during the life span of a project. State aid payable in the future, including aid payable in several instalments, shall be discounted, to its value at the moment it is granted.

(328) The permitted aid level is expressed in the Tables 7 to 20 as the lower of either the eligible costs (in nominal terms) or the funding gap (in discounted NPV terms). The Member States will ensure that the discounted value of the aid for each participating undertakings (using the weighted average cost of capital ("WACC") as a discount factor) will not exceed the notified funding gaps. In some cases, the notified State aid does not fully cover the funding gap of the respective individual projects. In those cases, the Member States concerned submit that the participating undertakings will proceed with the individual projects while seeking additional sources of funding. In some other cases, the Member States have not provided State aid in discounted figures, because the disbursement schedule with instalments over a certain period, has not yet been decided at national level, thereby making any discounting at this stage impractical.

([18]) Eligible costs are only those costs of the individual projects that comply with the requirements of the Annex to the IPCEI Communication. They, however, do not represent all costs required to conduct the R&D&I and FID activities concerned. The remaining portion of the costs required to conduct those activities, which are not considered eligible for public financing, will be absorbed by the participating undertakings.

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **AT&S** | [100 – 200] | [-200 – -100] | 110,0 | - |
| 2. | **AVL** | [50 – 60] | [-20 – -10] | 19,2 | - |
| 3. | **EEMCO** | [60 – 70] | [-30 – -20] | 28,8 | - |
| 4. | **IFX-AT** | [100 – 200] | [-60 – -50] | 83,9 | [50 – 60] |
| 5. | **NXP-AT** | [50 – 60] | [-20 – -10] | 14,4 | - |
| **Total** | | **491,1** | **-228,5** | **256,6** | **[50 – 60]** |

***Table 7: Austria – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Codasip** | [80 – 90] | [-40 – -30] | 42,8 | [30 – 40] |
| 2. | **Mycroft** | [10 – 20] | [-20 – -10] | 13,4 | [10 – 20] |
| **Total** | | 100,3 | -42,8 | 56,2 | 42,8 |

***Table 8: Czechia – State aid in million EUR***

| | Undertaking | *Million euro* | | |
|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** |
| 1. | **ADVA** | [90 – 100] | [-40 – -30] | 31,7 |
| 2. | **BLK** | [300 – 400] | [-300 – -200] | 235,8 |
| 3. | **Bosch-DE** | [1.500 – 2.000] | [-800 – -700] | 751,1 |
| 4. | **Cologne Chip** | [30 – 40] | [-30 – -20] | 21,8 |
| 5. | **Elmos** | [50 – 60] | [-50 – -40] | 43,9 |
| 6. | **Ericsson** | [90 – 100] | [-40 – -30] | 34,6 |
| 7. | **FCM** | [50 – 60] | [-40 – -30] | 32,8 |
| 8. | **FMC** | [30 – 40] | [-30 – -20] | 24,3 |
| 9. | **GF ([19])** | [800 – 900] | [-800 – -700] | 730,5 |
| 10. | **IFX-DE** | [900 – 1.000] | [-500 – -400] | 442,2 |
| 11. | **mi2** | [30 – 40] | [-40 – -30] | 37,7 |
| 12. | **Nokia-DE** | [300 – 400] | [-200 – -100] | 136,2 |
| 13. | **NXP-DE** | [600 – 700] | [-400 – -300] | 344,5 |
| 14. | **Osram** | [800 – 900] | [-400 – -300] | 323,6 |
| 15. | **R&S** | [20 – 30] | [-30 – -20] | 26,5 |
| 16. | **SGL** | [40 – 50] | [-30 – -20] | 27,0 |
| 17. | **Semikron-DE** | [90 – 100] | [-30 – -20] | 27,6 |
| 18. | **Trumpf Photonic** | [40 – 50] | [-40 – -30] | 31,8 |
| 19. | **UMS** | [50 – 60] | [-20 – -10] | 18,1 |
| 20. | **Wacker** | [100 – 200] | [-90 – -80] | 80,3 |
| 21. | **X-FAB-DE** | [80 – 90] | [-60 – -50] | 49,0 |
| 22. | **Zeiss** | [800 – 900] | [-500 – -400] | 411,1 |
| 23. | **ZF** | [1.500 - 2.000] | [-700 – -600] | 644,0 |
| **Total** | | **9.347,4** | **-4.510,7** | **4.506,0** |

***Table 9: Germany – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Cogninn** | [0 – 10] | [-10 – 0] | 1,2 | [0 – 10] |
| 2. | **Sunlight** | [10 – 20] | [-20 – -10] | 17,6 | [10 – 20] |
| **Total** | | 19,0 | -15,8 | 18,8 | 15,6 |

***Table 10: Greece – State aid in million EUR***

([19]) These eligible costs are distinct from those considered in SA. 102430 FR – Project Liberty - STMICROELECTRONICS S.R.L. (ST) – New semiconductor manufacturing plant by STMicroelectronics and GlobalFoundies (not yet published).

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Nokia-FI** | [100 – 200] | [-50 – -40] | 48,1 | [40 – 50] |
| **Total** | | **[100 – 200]** | **[-50 – -40]** | **48,1** | **[40 – 50]** |

***Table 11: Finland – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Airbus** | [60 – 70] | [-50 – -40] | 24,9 | [10 – 20] |
| 2. | **Aledia** | [300 – 400] | [-90 – -80] | 70,6 | [50 – 60] |
| 3. | **Continental-FR** | [100 – 200] | [-50 – -40] | 48,4 | [40 – 50] |
| 4. | **Lynred** | [80 – 90] | [-30 – -20] | 26,9 | [20 – 30] |
| 5. | **Orange** | [100 – 200] | [-50 – -40] | 50,1 | [40 – 50] |
| 6. | **Renault** | [100 – 200] | [-30 – -20] | 27,2 | [20 – 30] |
| 7. | **Soitec** | [600 – 700] | [-200 – -100] | 185,0 | [100 – 200] |
| 8. | **STM-FR ([20])** | [1.500 – 2.000] | [-400 – -300] | 452,0 | [300 – 400] |
| 9. | **Teledyne** | [40 – 50] | [-20 – -10] | 12,0 | [0 – 10] |
| 10. | **Valeo** | [100 - 200] | [-50 – -40] | 48,4 | [30 – 40] |
| 11. | **Vitesco** | [50 – 60] | [-20 – -10] | 18,5 | [10 – 20] |
| 12. | **X-FAB-FR** | [100 – 200] | [-50 – -40] | 49,5 | [40 – 50] |
| **Total** | | **3.553,8** | **-931,0** | **1.013,6** | **806,9** |

***Table 12: France – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **ADI** | [300 – 400] | [-90 – - 80] | 85,0 | [60 - 70] |
| **Total** | | **[300 – 400]** | **[-90 – -80]** | **85,0** | **[60 - 70]** |

***Table 13: Ireland – State aid in million EUR***

([20]) *Ibid.*

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **MEMC** | [100 – 200] | [-90 – -80] | 103,0 | [80 – 90] |
| 2. | **Menarini** | [60 – 70] | [-40 – -30] | 47,1 | [30 – 40] |
| 3. | **SIAE** | [100 – 200] | [-200 – -100] | 149,5 | [100 – 200] |
| 4. | **STM-IT ([21])** | [1.500 – 2.000] | [-600 – -500] | 686,8 | [500 – 600] |
| **Total** | | **2.271,0** | **-805,4** | **986,5** | **805,4** |

***Table 14: Italy – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **STM-MT** | [100 – 200] | [-70 – -60] | 60,0 | [40 – 50] |
| **Total** | | **[100 – 200]** | **[-70 – -60]** | **60,0** | **[40 – 50]** |

***Table 15: Malta – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **ASML** | [100 – 200] | [-100 – -90] | 96,0 | [70 – 80] |
| 2. | **Nearfield** | [40 – 50] | [-30 – -20] | 24,5 | [10 – 20] |
| 3. | **NXP-NL (6G)** | [60 – 70] | [-40 – -30] | 39,7 | [20 – 30] |
| 4. | **NXP-NL (Radar)** | [100 – 200] | [-50 – -40] | 59,5 | [30 – 40] |
| 5. | **Thermo Fisher** | [40 – 50] | [-30 – -20] | 37,0 | [20 – 30] |
| **Total** | | **475,0** | **-235,3** | **256,8** | **188,2** |

***Table 16: Netherlands – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Vigo** | [200 – 300] | [-200 – -100] | 102,9 | [70 – 80] |
| **Total** | | **[200 – 300]** | **[-200 – -100]** | **102,9** | **[70 – 80]** |

***Table 17: Poland – State aid in million EUR***

([21]) These eligible costs are distinct from those considered in SA. 103083 RRF -STMICROELECTRONICS S.R.L. (ST) – NEW SIC SUBSTRATES PLANT IN CATANIA (not yet published).

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Bosch-RO** | [60 – 70] | [-30 – -20] | 34,3 | [20 – 30] |
| 2. | **NXP-RO** | [100 – 200] | [-90 – -80] | 86,5 | [60 – 70] |
| 3. | **Continental-RO** | [200 – 300] | [-60 – -50] | 74,8 | [50 – 60] |
| **Total** | | **449,2** | **-163,7** | **195,6** | **145,4** |

***Table 18: Romania – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **Bizzcom** | [20 – 30] | [-30 – -20] | 22,4 | [20 – 30] |
| 2. | **Continium** | [60 – 70] | [-50 – -40] | 51,4 | [40 – 50] |
| 3. | **Tachyum** | [40 – 50] | [-30 – -20] | 27,8 | [20 – 30] |
| 4. | **Semikron - SK** | [30 – 40] | [-30 – -20] | 37,6 | [20 – 30] |
| **Total** | | **178,9** | **-119,2** | **139,3** | **119,2** |

***Table 19: Slovakia – State aid in million EUR***

| | Undertaking | *Million euro* | | | |
|---|---|---|---|---|---|
| | | **Eligible Costs (nominal)** | **Funding Gap (NPV)** | **State aid (nominal)** | **State aid (discounted/NPV)** |
| 1. | **IRVI** | [100 – 200] | [-80 – -70] | 104,3 | [70 – 80] |
| 2. | **KDPOF** | [50 – 60] | [-40 – -30] | 36,6 | [30 – 40] |
| 3. | **Semidynamics** | [70 – 80] | [-50 – -40] | 59,0 | [40 – 50] |
| 4. | **Openchip** | [400 – 500] | [-200 – -100] | 205,8 | [100 – 200] |
| **Total** | | **735,2** | **-293,2** | **405,7** | **293,2** |

***Table 20: Spain – State aid in million EUR***

(329) The Member State submit that the durations of the individual projects of the participating undertakings differ. The eligibility period (i.e., the period during which the costs that the undertakings can claim as eligible, should be incurred) is the following, per WS:

| WS | Start date | End date |
|---|---|---|
| SENSE | This WS starts at the earliest in 2022. | The last eligible year during the FID phase is planned at the latest 2032. |
| THINK | This WS starts at the earliest in 2022. | The last eligible year during the FID phase is planned at the latest 2031. |
| ACT | This WS starts at the earliest in 2022. | The last eligible year during the FID phase is planned at the latest 2029. |
| COMMUNICATE | This WS starts at the earliest in 2022. | The last eligible year during the FID phase is planned at the latest 2030. |

***Table 21: IPCEI ME/CT cost eligibility period***

*2.6.3. The aid instruments*

(330) The aid to be granted by all the Member States will take the form of direct grants.

## 2.7. Granting of the aid under the notified measures

(331) All of the Member States participating in IPCEI ME/CT have subjected the granting of State aid to the prior approval of the Commission.

(332) Pursuant to point 10 (a) of the IPCEI Communication, The Member States have further confirmed that the participating undertakings are not undertakings in difficulty as defined in the Guidelines on State aid for rescuing and restructuring non-financial undertakings in difficulty([22]).

(333) The Member States have furthermore committed to suspend the granting of the notified aid if the beneficiary still has at its disposal earlier unlawful aid that was declared incompatible by a Commission Decision (either as individual aid or aid under an aid scheme having been declared incompatible), until that beneficiary has reimbursed or paid into a blocked account the total amount of unlawful and incompatible aid and the corresponding recovery interest, pursuant to point 10 (b) of the IPCEI Communication.

(334) The Member States have also confirmed that aid under the IPCEI ME/CT will not be granted to the participating undertakings if it constitutes by itself, by virtue of the conditions attached to it or of its financing method, a non-severable violation of Union law, pursuant to point 10 (c) of the IPCEI Communication, in particular:

- granting of aid that is subject to the obligation for the beneficiary to have its headquarters in the Member State concerned or to be predominantly established in that Member State,
- granting of aid that is subject to the obligation for the beneficiary to use nationally produced goods or national services,
- aid restricting the possibility for the beneficiary to use the obtained R&D&I results in other Member States.

([22]) Guidelines on State aid for rescuing and restructuring non-financial undertakings in difficulty (OJ C 249, 31.7.2014, p. 1).

(335) Finally, the Member States have indicated that cumulation with other aid, de minimis aid ([23]) or Union funding will be allowed to cover the same eligible costs, provided that the total amount of public funding granted in relation to the same eligible costs does not exceed the most favourable funding rate laid down in the applicable rules of Union law, pursuant to point 35 of the IPCEI Communication.

### 2.8. Claw-back mechanism

(336) In order to further ensure that the aid is kept to the minimum necessary, the Member States have in their notification committed to introduce a claw-back mechanism, pursuant to point 36 of the IPCEI Communication. The basis for the claw-back mechanism will be *ex post* figures, which have been subject to annual approval by an independent auditor. For this purpose, separate analytical accounting will be required from the participating undertakings in the relevant Member State. The detailed conditions of the claw-back mechanism are explained in Annex I to this Decision.

(337) The claw-back mechanism for the individual projects of the participating undertakings only applies in case of a 'Surplus' including the actual State aid disbursements, as defined in Annex I to this Decision. To ensure, however, that the beneficiaries have an incentive to deliver their project in an efficient manner, a share of any potential 'Surplus' will remain with the participating undertakings.

(338) In line with previous case practice ([24]), the claw-back mechanism will apply at a minimum to participating undertakings having a notified aid amount, per Member State, above EUR 50 million. This threshold is appropriate as it ensures that the majority of participating undertakings, representing approximatively 86% of the total aid to be granted for the execution of IPCEI ME/CT will be subjected to the mechanism and at the same time avoids imposing burdensome administrative requirements on the relatively smaller projects.

(339) The Member States are required to report to the Commission on the implementation of the claw-back mechanism within two months after each application of that mechanism.

### 2.9. Transparency

(340) The Member States have in their notification committed to comply with the transparency and publication requirements of points 48 and 49 of the IPCEI Communication. In particular, the Member States have committed to publish in the Commission's transparency award module or on a comprehensive State aid website, at national or regional level, the full text of the individual aid granting decision and

([23]) Commission Regulation (EU) No 1407/2013 of 18 December 2013 on the application of Articles 107 and 108 of the Treaty on the Functioning of the European Union to de minimis aid (OJ L 352, 24.12.2013, p. 1).

([24]) SA.54794 (2019/N) and others - Important Project of Common European Interest (IPCEI) on Batteries, recital 196 (OJ C 292, 29.7.2022, p. 1); SA.55831 (2020/N) and others - Important Project of Common European Interest on European Battery Innovation (EuBatIn), recital 315 (not yet published); SA.64625 (2022/N) and others – Important Project of Common European Interest on Hydrogen Technology (Hy2Tech), recital 284 (not yet published); and SA.64631 (2022/N) and others – Important Project of Common European Interest on Hydrogen Industry (Hy2Use), recital 166 (not yet published);

its implementing provisions or a link to it, as well as all related information as specified in point 48 of the IPCEI Communication. ([25])

## 3. ASSESSMENT OF THE MEASURES

### 3.1. Presence of State aid pursuant to Article 107(1) TFEU

(341) According to Article 107(1) TFEU, "any aid granted by a Member State or through State resources in any form whatsoever which distorts or threatens to distort competition by favouring certain undertakings or the production of certain goods shall, in so far as it affects trade between Member States, be incompatible with the internal market".

(342) In order to qualify as State aid under Article 107(1) TFEU, the following cumulative conditions must be met: (i) the measure must be imputable to the State and financed through State resources; (ii) it must confer an advantage on its recipient; (iii) that advantage must be selective; and (iv) the measure must distort or threaten to distort competition and affect trade between Member States.

(343) The public support measures of the Member States will be financed with funds stemming from the respective State budgets. The measures therefore involve State resources and are imputable to the relevant Member States.

(344) The aid measures in the form of direct grants to the participating undertakings will relieve them from costs that they would have had to bear themselves under normal market conditions. By contributing to the financing of the R&D&I and FID activities with funds that would not have been obtained under normal market conditions, the aid measures confer an economic advantage on the aid beneficiaries over their competitors. These measures are granted only to the aid beneficiaries listed in section (44) on the basis of their individual projects. The aid measures are therefore selective.

(345) The aid beneficiaries involved in the relevant WS described above in section 2.2, operate in different sectors along the microelectronics and communications technologies value chain, namely for example semiconductors materials, specialised tools, chip designs to fabrication, new manufacturing processes and communication systems (e.g., 5G/6G, O-RAN etc). These are economic sectors open to intra-Union trade, both in terms of supply and demand. Therefore, the measures are liable to distort or threaten to distort competition and intra-Union trade, since they improve the competitive position of the beneficiaries compared to other undertakings with which they compete.

([25]) The Member States have notified the following websites for this purpose: www.bmk.gv.at/themen/innovation/internationales/ipcei/informationen.html (Austria), http://www.mpo.cz/ (Czechia), www.businessfinland.fi (Finland), https://www.europe-en-france.gouv.fr/fr/aides-d-etat (France), http://www.bmwi.de/ (Germany), http://www.espa.gr and http://www.ggb.gr/ (Greece), http://www.idaireland.com/ and https://webgate.ec.europa.eu/competition/transparency/public (Ireland), www.rna.it (Italy), https://stateaid.gov.mt/ (Malta), https://www.rijksoverheid.nl/onderwerpen/staatssteun (the Netherlands), www.sudop.uokik.gov.pl (Poland), http://www.mfe.gov.ro/ and http://www.economie.gov.ro/ (Romania), hppts://semp.kti2dc.sk and hppts://www.mhsr.sk (Slovakia), https://www.infosubvenciones.es/bdnstrans/es/index (Spain).

(346) In light of the foregoing, the Commission considers that the public support granted to the participating undertakings in the form of direct grants, as described within the framework of IPCEI ME/CT, qualifies as State aid within the meaning of Article 107(1) TFEU.

### 3.2. Legality of the aid measures

(347) The Member States submit that they shall not grant State aid to any of the participating undertakings before notification of the Commission's decision approving aid for the execution of IPCEI ME/CT. The granting of State aid will be governed by national funding agreements that are expected to be concluded following the Commission's decision (see recital (61)). By notifying the measures before putting them into effect, the Member States have fulfilled their obligations under Article 108(3) TFEU.

### 3.3. Assessment of the aid measures

#### *3.3.1. Applicable legal basis for assessment*

(348) In derogation from the general prohibition of State aid laid down in Article 107(1) TFEU, aid may be declared compatible by the Commission if it can benefit from one of the derogations enumerated in Article 107(2) and (3) TFEU.

(349) The Commission will assess the compatibility of the notified measures on the basis of Article 107(3)(b) TFEU, which concerns aid to promote the execution of an IPCEI. The criteria for the analysis of the compatibility with the internal market of State aid to promote the execution of IPCEIs are laid down in the IPCEI Communication. The Commission will examine whether IPCEI ME/CT satisfies the conditions laid down in the IPCEI Communication in the subsequent sections, following the structure of the Communication.

#### *3.3.2. Eligibility criteria*

(350) In order to be eligible for aid under Article 107(3)(b) TFEU, the notified measures must involve a project. That project must be of common European interest, and it must be important. These three criteria are considered below.

##### 3.3.2.1. Definition of a project

(351) According to point 13 of the IPCEI Communication, the Commission may consider eligible an "integrated project", that is to say, a group of single projects inserted in a common structure, roadmap or programme aiming at the same objective and based on a coherent systemic approach. The individual components of the integrated project may relate to separate levels of the supply chain but must be complementary and significantly add value in their contribution towards the achievement of the important European objective (see recitals (362) to (371)).

(352) The Member States, as explained in section 2.4, consider the notified IPCEI ME/CT to constitute an integrated project.

(353) The Commission finds that IPCEI ME/CT is designed in such a way as to contribute to the common objectives, formulated by the Member States and the participating undertakings, as described in section 2. As mentioned therein, the main aim of IPCEI

ME/CT is to create beyond global state-of-the-art microelectronics and connectivity solutions, aiming at enabling the digital transformation, by among other things advancing strategic technologies (e.g., system and chip design, EUV lithography, 3D integration, IC substrates, advanced packaging, photo masks, WBG materials etc.) with the use and integration of compound materials (e.g., SiC, GaN, InP, advanced photonics, SOI etc.), and enabling the most energy-efficient and resource-saving electronics systems and IT infrastructure.

(354) In particular, the Commission recognises the Member States' endeavour to jointly develop the microelectronics and communication technologies value chain, given its importance for the attainment of the Union's digital targets and digital transformation, as also illustrated in the various Union's communications and policy documents (see recitals (362) to (371)). Furthermore, the Commission notes that, in this framework, the Member States have developed different national strategies to address the microelectronic and communication technologies value chain with specific focuses and timelines. The Commission considers that the joint design of IPCEI ME/CT contributes to aligning the Member States' specific objectives and timelines towards achieving the Union objectives.

(355) Specifically, the Commission considers that IPCEI ME/CT integrates 68 individual projects based on coherent systemic approach. The presence of this coherent systemic approach is reflected in a common programme over the period from March 2021 to September 2021 (see recital (2)), prepared by the Member States, which resulted in the design of the Chapeau document. The Commission notes that the Chapeau document includes an overall work plan aimed at facilitating cross-border efforts towards common objectives.

(356) In particular, the Commission notes that the common programme established in the Chapeau document includes the definition of overall objectives at the level of IPCEI ME/CT (see section 2), articulated in specific objectives at the level of the four WS (see section 2.2), to be implemented and monitored under a common governance structure (see section 2.3).

(357) Furthermore, the organisation and work plan of the four WS is divided into different tasks, each of which consists of different components. The actions required in all of the tasks included within the organisation and work plan of the four WS add significant value for the achievement of IPCEI ME/CT's overall objectives (see sections 2.4.2, 2.4.3, 2.4.4 and 2.4.5).

(358) As described in section 2.4, each individual project is complementary to the other projects and significantly adds value in its contribution to the achievement of IPCEI ME/CT's objectives. In particular, the Commission notes that:

- the different individual projects in WS-SENSE are expected to design specialised technologies for different types of resilient sensing components, thereby developing and integrating new advanced sensors for dedicated applications (e.g., automotive, health, industry, space etc.) (see section 2.4.2);

- the different individual projects in WS-THINK plan at addressing a broad range of challenges from the development of equipment and materials, including substrates and EDA tools, to process and technology development, chip design and manufacturing. They furthermore target system level activities, notably architecture and SW over the full value chain, including the

development of secure, energy-efficient, and performant chip components for integration in systems (see section 2.4.3);

- the different individual projects in WS-ACT aim at developing technologies that go beyond the global state-of-the-art for Si smart power, WBG power electronics and compound materials, and discrete Si devices, with the monolithic and heterogeneous integration of SiC and GaN materials, with the purpose of improving the microelectronic systems' efficiency and the carbon footprint (see section 2.4.4);

- the different individual projects in WS-COMMUNICATE aim at addressing the development of communication systems (e.g., 5G/6G, O-RAN etc.) that will be implemented with the use of microelectronics components (e.g., CMOS, BiCMOS, photonic and packaging, etc.), thereby enabling an increase in the speed of networks and the transmission of larger amount of information and data (see section 2.4.5); and

- each WS, as illustrated in the respective sections 2.4.2 to 2.4.5) brings significant added value to the other, because of the use of specific technologies and common materials, which are expected to enable new technological and/or market perspectives. Furthermore, the complementarity between the four WS can be identified at material, technology, component and (sub-) system level, all of which representing parts of the microelectronics and communication technologies value chain and encompassing the entire IPCEI ME/CT ecosystem.

(359) In order to ensure the coherent implementation of IPCEI ME/CT, the Member States will establish a common governance structure, as described in section 2.3, under a SB, which will have the task of reviewing the progress and the results of IPCEI ME/CT and propose changes if necessary, giving specific attention to the benefit for the European society. The Commission will be represented in the SB as an observer. The Commission considers that IPCEI ME/CT's common governance structure will ensure that by joining their forces in the integrated IPCEI ME/CT, the Member States will be incentivised to implement and report as planned on their individual projects, establish the planned collaborations and enable the dissemination of spillover effects in a timely manner, without jeopardising the achievement of the common objectives.

(360) In view of the above, the Commission concludes that IPCEI ME/CT qualifies as an integrated project in the meaning of the IPCEI Communication, as its individual projects and WS are inserted in a common programme, aiming at the same objectives and based on a coherent systemic approach. Furthermore, the individual projects and WS are complementary and significantly add value in their contribution towards the achievement of the important common objective of establishing an innovative and sustainable microelectronics and communication technologies value chain in the Union.

#### 3.3.2.2. Common European Interest

(361) In order to establish that a project qualifies as being of common European interest, the IPCEI Communication sets out general cumulative criteria (section (a) below), as well as general positive indicators (section (b) below). In addition, the IPCEI

Communication sets out certain specific criteria depending on the type of project (section (c)).

(a) General cumulative criteria (section 3.2.1 of the IPCEI Communication)

*Important contribution to the Union's objectives*

(362) According to point 14 of the IPCEI Communication, the project must represent a concrete, clear and identifiable important contribution to the Union's objectives or strategies and must have a significant impact on sustainable growth, for example by being of major importance among others for the European Green Deal, the New Industrial Strategy for Europe and its update, the Next Generation EU, the new European Research Area for research and innovation, the new Circular Economy Action Plan, or the Union's objective to become climate neutral by 2050.

(363) The objective to accelerate Europe's digital transformation was already set in the past decade with the *Digital Single Market* ([26]), whereas specific actions were defined in the subsequent strategy for *Shaping Europe's digital future* ([27]). Furthermore, in its *Digital Compass Communication*, the Commission laid out its vision for 2030 to empower citizens and businesses through digital transformation and enable Europe to become digitally resilient and sovereign. ([28])

(364) With the *Digital Decade Policy Programme*, the Union sets out a monitoring and cooperation mechanism designated to among other things create an environment favourable to innovation and investment by setting a clear direction for the digital transformation of the Union and for the delivery of digital targets by 2030 (e.g., related to digital skills for population and businesses, secure, resilient, performant and sustainable digital infrastructures, digital transformation of businesses and digitalisation of public services), on the basis of measurable indicators. ([29])

(365) The *Next Generation EU* stimulus package has been adopted as a temporary instrument designed to boost the recovery of Member States from the COVID-19 pandemic by addressing among others, the transition to a digital economy. ([30]) The *Resilience and Recovery Facility ("RRF")* for Europe constitutes a centrepiece of the Next Generation EU. ([31]) The RRF Regulation requires each Member State to

([26]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *A Digital Single Market Strategy for Europe*, COM(2015) 0192 final, 6 May 2015.

([27]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *Shaping Europe's digital future*, COM(2020) 67 final, 19 February 2020.

([28]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *2030 Digital Compass: the European way for the Digital Decade*, COM(2021) 118 final, 9.3.2021.

([29]) Decision (EU) 2022/2481 of the European Parliament and of the Council of 14 December 2022 establishing the Digital Decade Programme 2030, OJ L 323, 19.12.2022.

([30]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *Europe's moment: Repair and Prepare for the Next Generation*, COM(2020) 456 final, 27.5.2020.

([31]) Regulation (EU) 2021/41 of the European Parliament and of the Council of 12 February 2021 establishing the Recovery and Resilience Facility, OJ L 57, 18.2.2021, p. 17-75.

dedicate at least 20% of its recovery and resilience plan's ("RRP") total allocation to measures contributing to the digital transition or to addressing the challenges resulting therefrom. IPCEI ME/CT projects will be partly funded by the RRF.

(366) All of the above legislative initiatives supplement the Commission's Communication that sets out a *European Green Deal* for the Union and its citizens, where the Commission emphasised that the Union should leverage the potential of the digital transformation, as digital technologies and new methods and processes are critical enablers for reaching the European Green Deal objectives for reducing greenhouse gas emission by at least 55% by 2030, compared to 1990 levels and ensuring climate neutrality by 2050. ([32]) In addition, the *Green Deal Industrial Plan for Net Zero Age* calls for European standards to promote the roll-out of clean and digital technologies and provide Union industries an important competitive advantage, including at global level. ([33])

(367) The Commission considers that IPCEI ME/CT will contribute to fulfilling the objectives laid down in the various Union initiatives mentioned above by:

- bringing together in an integrated project 56 participating undertakings from 14 Union Member States, with 32 associated participants and approximately 600 indirect partners, aiming for the creation of an ecosystem of innovative start-ups, SMEs, large undertakings and ROs/Universities;

- stimulating collaborative interactions between the direct participants, with the aim towards developing quickly the expected technologies with the use of the different technology elements required by the different collaborators (e.g., equipment, materials, masks, device designs and processes etc.), and facilitating the creation of the microelectronics and communication technologies ecosystem;

- bringing together Member States that have adopted the goal of the *Digital Decade Policy Programme* within their national strategies and identified advanced technology nodes as a key ingredient to achieve this goal;

- offering a structured framework to the Member States and the participating undertakings to mobilise funds from the RRF in a coordinated manner;

- addressing the technological performance, sustainability and societal challenges of the next decade, putting emphasis on the reduction of energy consumption within the microelectronics (i.e., power electronics, sensor systems, advanced node processors and memory systems) and the communication technologies domains; and

([32]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *The European Green Deal*, COM(2019) 640 final, 11.12.2019.

([33]) Communication from the Commission, to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *A Green Deal Industrial Plan for the Net-Zero Age*, COM(2023) 62 final, 1.2.2023.

- addressing the resilience of the microelectronics and communication technologies value chain by implementing in a coordinated manner appropriate industry standards to accelerate the Union's digital transformation.

(368) The Commission furthermore notes that IPCEI ME/CT will also contribute to *the new ERA for Research and Innovation* ([34]) and *the New European Innovation Agenda ([35])*. In this context, IPCEI ME/CT will:

- host R&D&I activities for innovative and sustainable microelectronics and communication technologies, with the result of unlocking the full technological potential of the entire microelectronics and communication technologies value chain in the Union, from materials to system integration (see recital (15)). Accordingly, the individual projects of the participating undertakings will cover all the elements of the value chain needed to develop, produce, and integrate these technologies, notably manufacturing and test equipment, materials, processes, design capacities and competences, in the areas of notably, power semiconductors, low-power digital electronics, micro controllers, image sensors, RF electronics, integrated photonics and MEMS;

- contribute to the transfer of microelectronics and communication technologies-related knowledge to new or improved applications and different output sectors;

- support the training and strengthen the science, technology, engineering and mathematics education of highly skilled staff; and

- help coordinate microelectronics and communication technologies-related activities across Europe in order to create an integrated Union ecosystem, thereby delivering on the ambition of IPCEI ME/CT.

(369) Particularly it is expected that the IPCEI ME/CT will trigger significant R&D&I and FID investments by the participating undertakings, as it is shown in Table 22, which provides an overview of the main progress KPIs to be achieved until the end of IPCEI ME/CT:

([34]) Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, *A new Era for Research and Innovation*, COM(2020) 628 final, 30.9.2020.

([35]) Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, *A new European Innovation Agenda*, COM(2022) 332 final, 5.7.2022.

| KPI | Description | Quantified objective |
|---|---|---|
| **Design Centres** | Cumulated number of new design centres | 10 |
| **FID implementation** | Number of FID project phases expected to start | 321 |
| **Cybersecurity** | Number of new products or solutions adopting cybersecurity measures at chip and/or SW level realised in the various WS | 79 |
| **New technologies** | Number of new technologies for downstream industry (automotive, industrial, medical, etc.) reaching TRL 6 or above | 246 |
| **New products** | Number of new products for downstream industry (automotive, industrial, medical, etc.) reaching TRL 6 or above | 419 |
| **Pilot lines** | Number of new pilot lines for R&D&I / FID | 92 |
| **Manufacturing equipment** | Number of new semiconductor manufacturing and testing equipment / CAD tools produced | 17 |

**Table 22: Overview of the progress KPIs**

(370) As regards the contribution of IPCEI ME/CT to the *New Industrial Strategy for Europe* ([36]), the Commission acknowledges the importance of IPCEI ME/CT for supporting significant investments in the Union's microelectronics and communication technologies value chain and that IPCEI ME/CT is expected to contribute, according to estimates provided by the Member States, to job creation by creating approximately 8 800 direct jobs over its implementation.

(371) Based on the foregoing (recitals (367) to (370)), the Commission considers that IPCEI ME/CT will deliver on its overall objectives (see recital (10)) and contribute significantly to fostering R&D&I, especially through the substantial investments undertaken by the participating undertakings and the planned collaborations. The Commission therefore concludes that IPCEI ME/CT will provide an important contribution, in a concrete, clear and identifiable manner, to one or more Union objectives and has in particular a significant impact on sustainable growth across the Union.

*Important market failures*

(372) According to point 15 of the IPCEI Communication, the project must demonstrate that it is designed to overcome important market or systemic failures, preventing it from being carried out to the same extent or in the same manner in the absence of the aid, or societal challenges, which would not otherwise be adequately addressed or remedied.

(373) The Commission's assessment focused on the important market failures notified by the Member States for each individual project, by identifying first the existence of such market failures and elaborating at a second step on how each individual project addresses it specifically. This allowed the Commission to define the overarching market failures specific to IPCEI ME/CT.

([36]) Communication from the Commission to the European Parliament, the European Council, the Council, the European Economic and Social Committee and the Committee of the Regions, *A New Industrial Strategy for Europe*, COM (2020) 102 final, 10.3.2020.

(374) First, the integrated, coordinated and simultaneous nature of the individual projects in IPCEI ME/CT is expected to address coordination problems in the development of innovative technologies and products, by aligning the incentives of multiple actors with diverging interests along the whole value chain.

(375) When the profitability of various projects is interdependent, multiple actors may end up underinvesting, if they are not able to coordinate and invest simultaneously, e.g., in order to commercialise a new technology or innovation. The strategic interaction between the various necessary actors may require State intervention to coordinate actions and align incentives, in order to accelerate those interdependent investments.

(376) IPCEI ME/CT will address coordination problems, by aligning incentives of a large number of undertakings, often with diverging interests, involved in IPCEI ME/CT, thereby fostering the entire microelectronics and communication technologies value-chain through the build-up of pilot-lines, complex chip design and production capabilities using European innovative technologies and products designed and developed during a joint effort. Examples include:

- developing and deploying WBG semiconductors for automotive applications by aligning incentives of wafer manufacturers, foundries, IDMs, tier-ones, research labs and end-users. The necessary new solutions need to be developed at all levels of the value chain quickly and in parallel, thereby addressing the challenges of electromobility (e.g., expand the range of the car and prolong the lifecycle of the battery) and AD (e.g., security, reliability), meeting the aims of green and digital transitions and improving the market acceptance of those products;

- developing and deploying next generation of telecommunication equipment and system such as photonics technology, coordinating actions of undertakings at different levels of the value chain, from the production of compound materials and wafers to the packaging and testing of components; and

- the advanced packaging projects supported in the IPCEI ME/CT will help overcome the challenge caused by the concentration of outsourced semiconductor assembly and test ("OSAT") services outside Europe. European SME's and start-ups willing to access OSAT's services have difficulty to be competitive with much larger companies and have a very limited range of providers in Europe. Consequently, the European actors, in particular the smaller ones, need to seek alternative suppliers of the necessary equipment, and coordinate with them the development of the tools, adapted to their flexibility needs and scale. The objective is to move away from the current semiconductor assembly and test services provided at large-scale, and develop smaller, highly flexible advanced packaging services in Europe, which would help European players implement and test even small innovative projects.

(377) Second, the individual projects in IPCEI ME/CT are expected to address the problem of asymmetric information of innovative projects along the entire microelectronics and communication technologies value chain, showing the willingness of Member States to support related projects.

(378) The presence of asymmetric information may lead to a situation where innovators may face difficulties convincing investors of the prospects of their projects in light of the risks and uncertainties involved, the low technology readiness level and the lack

of expertise in such a highly specialised market segment. State aid may complete this gap by raising access to finance of start-ups and SME's, raising the technological readiness of projects at a level compatible with investor's interest, thereby contributing to advocate for the relevance of the project to investors.

(379) Furthermore, the participating undertakings, with State aid, will be capable of securing cooperation with suitable technology providers (e.g., foundry), and demonstrate the validity of their planned technology.

(380) IPCEI ME/CT seeks to address problems with respect to asymmetric information, for instance by:

- providing the possibility for SMEs and start-ups to access or implement beyond the state-of-the art pilot-lines with the adequate technology. Without that access, creating prototypes and demonstrating the innovative and commercial potential of smaller projects to prospective investors would be considerably limited, if not impossible; and

- providing innovative technologies, such as photonics on silicon, advanced nodes with associated memories, or new WBG semiconductor technologies to start-up and SMEs, facilitating their prototyping activities and increasing their technology readiness levels to the degree acceptable for potential investors.

(381) Third, the individual projects in IPCEI ME/CT are expected to address positive externalities of innovation efforts, not fully internalised by the beneficiaries. Where individual projects provide benefits to society that are not fully captured by the undertakings, the latter's private rate of return may not be sufficiently attractive for each project to be funded fully privately, even though the overall benefits of that project would justify the investment from a societal perspective. In the presence of positive externalities, the social rate of return on the R&D&I investment made by undertakings is higher than the undertakings' private return from the R&D&I investment. This leads to the underinvestment (or underproduction) in innovative technologies along the microelectronics and communication technologies value chain, from the social perspective, which justifies the need for State intervention. State aid may bridge this gap and ensure a level of innovation closer to a socially optimal level.

(382) Projects under IPCEI ME/CT will address such positive externalities generating benefits from innovation efforts going beyond undertaking-specific benefits and fuelled by interactions between undertakings involved, for instance by:

- creating jobs and training opportunities along the different levels of the microelectronics and communication technologies value chain and across different countries in Europe, with the aim towards stimulating regional employment not only in undertakings that indirectly benefit from the projects under IPCEI ME/CT, but also in the local economy more generally;

- creating offer of more cost-efficient and performant microelectronics components and systems enabling solutions necessary for the digital transformation, thereby contributing to the increased digital inclusion and development of digital services and their wide availability; and

- accepting passive dissemination of knowledge and results to other market participants, including those beyond the beneficiaries' own sectors of activities. In other words, this dissemination will occur spontaneously and beyond the control of the relevant undertakings e.g., through the natural mobility of employees.

(383) Lastly, the individual projects in IPCEI ME/CT will contribute to addressing a market failure in the form of negative externalities, by developing highly innovative solutions and technologies to production of microelectronics components towards less energy-consuming and less polluting solutions.

(384) Negative externalities may occur when a firm does not bear the full cost of the harm they impose on society. Environmental negative externalities, for instance, lead to the use of excessively polluting technologies. In this context, the objective of State aid would be to promote the development and/or adoption of "cleaner" technologies and processes.

(385) Undertakings of the microelectronics and communication technologies sectors compete globally with competitors subject to different sets of regulation that is not aligned. The Commission notes that despite the microelectronics manufacturing environmental footprint, no common global environmental policy exists in the sectors to reduce the environmental impact of a product lifecycle or even to differentiate the product based on its environmental sustainability. As a result, in the absence of level playing field and of State aid, the companies lack incentive to invest on improving the environmental impact of their products and processes.

(386) The individual projects under IPCEI ME/CT will address negative environmental externalities, for instance by:

- undertaking research on the design and production of microelectronics components towards less energy-consuming and less polluting solutions, reducing the use of hazardous chemicals and metals, and using recyclable and/or recycled water, packaging or materials;

- optimising manufacturing processes in order to increase the operational life of the devices, and reducing the replacement rate and the need for new products; and

- improving recyclability of the components and systems in an energy- and environment-friendly way and re-integration of recycled raw materials, especially rare metals, in the microelectronics and communication technologies value chain.

(387) In addition to the market failures identified above, the individual projects in IPCEI ME/CT will contribute to strengthening Union's microelectronics and communication technologies ecosystem, significantly reducing its external dependencies, for instance by providing opportunities to fabless companies to access advanced technologies. The individual projects under IPCEI ME/CT plan to addressing issues of security of supply as Europe may face security risks associated with dependency on non-European suppliers of microelectronics and communication products and components. This is the case of participating undertakings under IPCEI ME/CT that on their own would not be willing to invest in novel production methods

in Europe to address issues of security of supply, thereby motivating the need for market intervention.

(388) Based on the above, the Commission concludes that the eligibility condition of IPCEI ME/CT demonstrating that it is designed to overcome important market failures, has been fulfilled.

Member States involved

(389) Point 16 of the IPCEI Communication requires that at least four Member State must ordinarily be involved in an IPCEI and its benefits must not be confined to the financing Member States but extend to a wider part of the Union, where as those benefits must be clearly defined in a concrete and identifiable manner. The Commission notes that the notified IPCEI ME/CT involves 14 Member States, i.e.: Austria, Czechia, Finland, France, Germany, Greece, Ireland, Italy Malta, The Netherlands, Poland, Romania, Slovakia and Spain, and, as shown in recitals (391) to (401), its benefits are widely spread and defined in a concrete and identifiable manner It is therefore concluded that the eligibility condition of point 16 of the IPCEI Communication is fulfilled.

Open procedure for Member States

(390) On 7 December 2020, 22 Member States signed a joint Declaration on a European Initiative on Processors and semiconductor technologies in which they committed to launch IPCEI on IPCEI ME/CT. In line with point 17 of the IPCEI Communication, the signatory Member States invited all other Member States to join this initiative, open to countries willing to participate in the design of IPCEI on IPCEI ME/CT. Therefore, the Commission concludes that the eligibility condition of ensuring a genuine opportunity for all interested Member States to participate in IPCEI ME/CT has been fulfilled.

Positive spillover effects

(391) Point 18 of the IPCEI Communication, requires that an IPCEI must benefit the European economy or society via positive spillover effects. In particular, the benefits of the project must not be limited to the undertakings or to the sector concerned but must be of wider relevance and application to the economy or society in the Union through positive spillover effects (such as having systemic effects on multiple levels of the value chain, or up- or downstream markets, or having alternative uses in other sectors or modal shift) which are clearly defined in a concrete and identifiable manner.

(392) The IPCEI Communication requires for spillover effects to be identified at all of the following levels: beyond the Member States ("economy or society in the Union"); beyond the aid beneficiaries ("not be limited to the undertakings"); beyond the sector(s) in which the aid beneficiaries are active ("[…] or to the sector concerned").

(393) In view of the commitments for spillover effects as submitted by the Member States for each individual project, the Commission observes that different dissemination levels, ranging from awareness to exploitation, are proposed to ensure the translation of developments and outputs into new findings and market opportunities. The objective is to reach a wide range of potential users and uses amongst research, social, investment and policy makers. In addition, the Commission observes that

several of the notified individual projects benefitted from earlier R&D&I work performed during the activities of the Key Digital Technologies Joint Undertaking ([37]) and other relevant EU initiatives funded under Horizon Europe. ([38]) The Commission expects that the spill-over commitments proposed by the participating undertakings will facilitate the exchange of information and dissemination of results, cooperation and synergies with the activities of the said programmes.

(394) As regards spillover effects for non-IP protected results of R&D&I and FID activities, the Member States have provided an extensive list of activities (described in section 2.5.1) illustrating that the results of IPCEI ME/CT are not limited to the participating undertakings and the Member States concerned, but will be disseminated to the whole scientific community and be of wider relevance and application to different economic sectors. For example, the Commission recognises that involvement in conferences and events as speakers, contributors, or participants will contribute to the dissemination of the knowledge, skills and results obtained through the IPCEI ME/CT in the sense that participation in these events is typical of all key actors (i.e., undertakings, ROs, universities, etc.) of the microelectronics and communication technologies value chain, as they provide an opportunity to exchange on the specific results produced by each individual project and the technological advancements achieved (see section 2.5.1.2). Moreover, the establishment of collaborations with numerous and various associated participants and indirect partners (see sections 2.5.4 and 2.5.5), will enhance the dissemination effort.

(395) The Commission also notes the significant effort undertaken by the participating undertakings to spread and share knowledge and results through publications in peer-reviewed journals (see section 2.5.1.4) and in increasing links with the academic world, including through collaborations for the implementation of IPCEI ME/CT, but also through a significant sponsorship of Ph.D. and MSc degrees and university chairs related to technologies developed under IPCEI ME/CT (see recital (241) and (245) to (246)). This is particularly important to ensure that the knowledge and individual project's results of IPCEI ME/CT are transmitted to the next generations and that the future workforce can acquire the skills and knowledge that will be needed in the future. This is, furthermore, corroborated by the commitments undertaken by all of the participating undertakings to provide training activities in collaboration with ROs and universities, targeting professional and researchers (see recital (248)).

(396) As regards spillover effects for IP-protected results of R&D&I (see section 2.5.2), the Commission considers that the Member States have adequately described the dissemination activities and the commitments undertaken by the participating undertakings to spread those results as widely as possible to interested parties, e.g. SMEs or ROs, the scientific community and across economic sectors beyond the Member States involved, among other things, through non-exclusive licensing based on FRAND conditions, without jeopardising the objectives of IPCEI ME/CT. Thus,

([37]) https://european-union.europa.eu/institutions-law-budget/institutions-and-bodies/search-all-eu-institutions-and-bodies/key-digital-technologies-joint-undertaking_en#:~:text=Overview,electronic%20components%20and%20systems%20sector

([38]) https://research-and-innovation.ec.europa.eu/funding/funding-opportunities/funding-programmes-and-open-calls/horizon-europe_en

the IP-protected results will not only benefit the participating undertakings, but will go beyond the undertakings generating those results during IPCEI ME/CT.

(397) In line with the commitments provided by each participating undertaking (see recital (249)), the setting of the licence fees will be fixed in the respective cooperation contracts between the participating undertakings and the interested parties. This dissemination will provide interested parties with the possibility to reap the benefits of the R&D&I activities undertaken by IPCEI ME/CT across the WS. Through access on FRAND terms to IP-protected results of R&D&I stemming from individual projects falling within IPCEI ME/CT, it can be expected that interested parties will be able to exploit the results of IPCEI ME/CT in different applications, in up- or downstream markets across the Union, increasing therefore their technological expertise and their own research activities, improving their own equipment, materials and processes and having the opportunity to develop new products or establish new collaborations.

(398) As far as particular spillover effects of FID activities are concerned, the Commission considers that, on the basis of the information provided by the Member States (described in section 2.5.3), the FID activities are expected to lead to significant spillover effects in downstream markets. IPCEI ME/CT will enable the participating undertakings to develop new product applications and designs and acquire specific skills and know-how, which can be used in cooperation with third parties within or outside IPCEI ME/CT. IPCEI ME/CT will also provide hands-on training activities, access to next generation microelectronics and communication-related technologies and know-how, to other interested large undertakings, as well as to SMEs and ROs that want to develop new knowledge and applications, considering the entire lifecycle of these technologies. These parties are expected to benefit from specific knowledge sharing and early access to the latest technologies available, and may thus be able to reduce the development time of their own applications.

(399) In this regard, the Commission notes that some of the participating undertakings have committed to provide design/testing kits for electronic components and products and to granting access to R&D&I lab production lines for SMEs (including start-ups) and ROs, which are not familiar with the respective technologies and which do not have the capability to build up their own lab system (see section 2.5.3, for example recitals (251), (289), (291), (297), (299), (304), (307) and (310)), in order to carry out their own research and testing and develop new applications. Both the design/testing kits and the lab production lines are in principle planned to function as start-up incubators for knowledge-based ventures in areas related to the operation of microelectronics and communication technologies, for different applications within the value chain, thereby creating spillover effects in the downstream markets and the scientific community.

(400) Based on the description of the positive spillover effects generated by IPCEI ME/CT as presented in section 2.5, the Commission considers that the benefits of IPCEI ME/CT are clearly defined in a concrete and identifiable manner and the Member States have adequately shown how IPCEI ME/CT benefits interested parties beyond those directly involved in IPCEI ME/CT and beyond the Member Stated and economic sectors concerned. In addition, the Commission notes that at both integrated and national governance levels IPCEI ME/CT will monitor the correct implementation of the committed dissemination activities and spillovers of the

participating undertakings (see recitals (53) and (61)) in compliance with the point 52 of the IPCEI Communication and the national funding agreements.

(401) Therefore, in view of the above the Commission considers that this eligibility condition is satisfied, in accordance with point 18 of the IPCEI Communication.

Co-financing by the aid beneficiaries

(402) As required by point 19 of the IPCEI Communication, the project must involve important co-financing by the beneficiaries. The Commission estimates that the total financing needs for the implementation of the beneficiaries' projects are approximately EUR 12.3 billion in total. It is therefore concluded that the eligibility condition of point 16 of the IPCEI Communication is fulfilled.

Principle of 'do no significant harm'

(403) Point 20 of the IPCEI Communication requires Member States to provide evidence as to whether the project complies with the principle of 'do no significant harm' within the meaning of Article 17 of Regulation (EU) 2020/852 (the "Taxonomy Regulation"), or other comparable methodologies. ([39])

(404) Article 17 of the Taxonomy Regulation defines what constitutes 'significant harm' for the six environmental objectives covered by the Taxonomy Regulation, taking into account the life cycle of the products and services provided by an economic activity including evidence from existing life cycle assessments:

- an activity is considered to do significant harm to climate change mitigation if it leads to significant GHG emissions;
- an activity is considered to do significant harm to climate change adaptation if it leads to an increased adverse impact of the current climate and the expected future climate, on the activity itself or on people, nature or assets;
- an activity is considered to do significant harm to the sustainable use and protection of water and marine resources if it is detrimental to the good status or the good ecological potential of bodies of water, including surface water and groundwater, or to the good environmental status of marine waters;
- an activity is considered to do significant harm to the circular economy, including waste prevention and recycling, if it leads to significant inefficiencies in the use of materials or in the direct or indirect use of natural resources, or if it significantly increases the generation, incineration or disposal of waste, or if the long-term disposal of waste may cause significant and long-term harm to the environment;
- an activity is considered to do significant harm to pollution prevention and control if it leads to a significant increase in emissions of pollutants into air, water or land, as compared with the situation before the activity started; and

([39]) Regulation (EU) 2020/852 of the European Parliament and of the Council of 18 June 2020 on the establishment of a framework to facilitate sustainable investment (OJ L 198, 22.6.2020, p. 13).

- an activity is considered to do significant harm to the protection and restoration of biodiversity and ecosystems if it is significantly detrimental to the good condition and resilience of ecosystems, or detrimental to the conservation status of habitats and species, including those of Union interest.

(405) In order to assess compliance with point 20 of the IPCEI Communication, the Commission requires Member States to provide evidence that demonstrates that the individual projects comply with the above-mentioned six environmental objectives of the Taxonomy Regulation, by reference in particular to the screening criteria developed in Commission Delegated Regulation (EU) 2021/2139 of 4 June 2021 supplementing Regulation (EU) 2020/852 of the European Parliament and of the Council for determining the conditions under which an economic activity qualifies as contributing substantially to climate change mitigation or climate change adaptation and for determining whether that economic activity causes no significant harm to any of the other environmental objectives (the "Delegated Regulation") ([40]).

(406) The Commission assessed the environmental impact of all of the individual projects against the six environmental objectives set out in Article 9 of the Taxonomy Regulation. For all individual projects included in the IPCEI ME/CT the Commission finds the following:

(407) Concerning climate change mitigation, the Commission finds that the Member States have shown, that advancements related to climate change mitigation are mainly expected to be achieved by energy and/or power reduction, as well as by an increase in energy efficiency of the technology or devices developed under IPCEI ME/CT, which, in turn, is expected to lead to a reduction of emissions for the final applications. For instance, IPCEI ME/CT envisages technological innovation in CMOS, BiCMOS, photonics and packaging, thereby supporting more energy efficient optical and wireless communication systems that are planned to contribute to reducing greenhouse gas emissions significantly. Additionally, on the basis of the notified information, the Commission observes that the participating undertakings have taken into consideration in their planned measures the positive environmental impacts of the resulted technologies or devices, due to improvements in the production and fabrication processes, including lower material and less energy consumption, as well as the reduction of waste. The Commission furthermore observes that the Member States have committed to monitor the amount of electric energy from green energy sources consumed by the production processes under the IPCEI ME/CT, as well as the $CO_2$ emissions caused by the production processes.

(408) Concerning climate change adaption, the Commission finds that no negative effects are foreseeable. The reduction of consumption and increase in energy efficiency is a major criterion for all of the individual projects selected for IPCEI ME/CT. As the microelectronics and communication technologies value chain is geographically fragmented, the environmental costs resulting from long range transport is very high. Therefore, the implementation of a logistics circuit refocusing many of the different steps of the value chain within Europe is expected to reduce the overall carbon footprint of the value chain. As an example, in the case of WBG components made on substrates manufactured, designed, assembled, and packaged in Europe, before being integrated in power modules, the estimated distance covered could go from 40

([40]) OJ L 442, 9.12.2021.

000 km (counterfactual scenario) to typically 4 000 km, thereby directly significantly reducing the associated emissions during transport.

(409) Concerning the sustainable use and protection of water and marine resources, the Member States have demonstrated that the individual projects, plan to reduce the water consumption, as well as the wastewater, and apply specific wastewater treatment. The Commission furthermore notes that for those individual projects, where the use of water and marine resources constitute part of the relevant activities, the Member States have committed to evaluate the water consumed in the manufacturing process under the IPCEI ME/CT, as well as the water recycling rate.

(410) The Member States have also shown that the individual projects under IPCEI ME/CT will contribute to the circular economy, including waste management, thereby fulfilling the required standards of preventing significant harm. A main challenge consists in minimising the waste, considering the entire life cycle/value chain of the electronics ecosystem. To this end, IPCEI ME/CT involves activities that aim at optimising manufacturing processes, thereby increasing the operational life of the devices. For instance, in some cases the participating undertakings, will focus on the reduction of the replacement rate and the exploitation of eco-sustainable materials, by exploiting green technologies and the use of recyclable materials

(411) The Commission considers that it is unlikely that the activities carried out under the IPCEI ME/CT will lead to a significant increase in emissions of pollutants into air, water or land. Several participating undertakings have outlined that there is no connection between their activities and the pollution prevention and control of air, water and land. Furthermore, in some cases, the participating undertakings plan to carry out research on the design and production of microelectronics components towards less energy-consuming and less polluting solutions, by reducing the use of hazardous chemicals and metals, using recyclable and/or recycled water, packaging or materials, optimising manufacturing processes.

(412) Finally, the Commission verified that the protection and restoration of biodiversity and ecosystems does not have a significant negative impact on the protection and restoration of biodiversity and ecosystems. In general, the protection and restoration of biodiversity and ecosystems play a minor role for the individual projects in IPCEI ME/CT. Most of the individual projects are expected to have no or just an insignificant impact on the protection and restoration of biodiversity and ecosystems. In those cases where this criterion applies, the participating undertakings have provided information showing that they aim towards paying particular attention during building processes, for instance, by reducing waste and increase recycling efforts, or by decreasing material and water, as well as energy usage.

(413) In view of the above, the Commission considers that this eligibility condition is satisfied, in accordance with point 20 of the IPCEI Communication.

Conclusion

(414) Based on all of the above considerations, the Commission considers that the general cumulative criteria for eligibility of the notified IPCEI ME/CT for aid under Article 107(3)(b) TFEU are met.

(b) General positive indicators (section 3.3.3 of the IPCEI Communication)

Involvement of the Commission in the design

(415) The Commission facilitated the emergence of IPCEI ME/CT and helped enhance coordination between Member States in the project by having participated and contributed during the period preceding the pre-notifications in several technical meetings with open invitations for all Member States interested in participating in IPCEI ME/CT. This is consistent with point 21(a) of the IPCEI Communication.

Involvement of the Commission in the governance

(416) As described in detail above under section 2.3, the governance structure of IPCEI ME/CT involves the Commission through participation into the SB. This is consistent with point 21(c) of the IPCEI Communication

Important collaborative interactions

(417) The Member States provided detailed information (see section 2.4.4) describing how each individual project creates important collaborative interactions in terms of the number of partners, involvement of undertakings participating in the same and different TF and the involvement of undertakings of different sizes.

(418) The Commission takes note of the number of collaborations within each and across the different WS, as illustrated in table 23 and further elaborated in section 2.4.6 (collaborations within IPCEI ME/CT), section 2.5.4 (collaborations with associated participants) and section 2.5.5 (collaborations with indirect partners). It is evident from the information submitted by the Member States that, all of the participating undertakings in IPCEI ME/CT are involved in multiple cross-border and national collaborations. The Commission considers that such collaborations are in line with point 21(d) of the IPCEI Communication.

| WS | Number of direct collaborations | | | Number of collaborations between associated and direct participants | | | Number of indirect collaborations intra WS |
|---|---|---|---|---|---|---|---|
| | Intra WS | Inter WS | | Intra WS | Inter WS | | |
| | Number of collaborations | WS | Number of collaborations | Number of collaborations | WS | Number of collaborations | |
| WS-SENSE | 26 | WS-THINK | 18 | 20 | WS-THINK | 2 | 201 |
| | | WS-ACT | 11 | | WS-ACT | 4 | |
| | | WS-COMMUNICATE | 16 | | WS-COMMUNICATE | 3 | |
| WS-THINK | 61 | WS-ACT | 8 | 21 | WS-ACT | 4 | 234 |
| | | WS-COMMUNICATE | 15 | | WS-COMMUNICATE | 2 | |
| WS-ACT | 57 | WS-COMMUNICATE | 3 | 21 | WS-COMMUNICATE | 3 | 160 |
| WS-COMMUNICATE | 58 | - | - | 29 | - | - | 296 |
| Total | 202 | | 71 | 91 | | 18 | 891 |
| | 273 | | | 109 | | | |

***Table 23: Summary of the different inter and intra WS collaborations***

Co-funding or co-financing from a Union fund

(419) The Commission acknowledges that most of the Member States will be using for all of their projects co-funding or co-financing from the European Regional Development Fund, the Just Transition Fund, the Innovation Fund and/or the RRF.

The inclusion of co-funding or co-financing of individual projects within IPCEI ME/CT is consistent with point 21(e) of the IPCEI Communication.

Significant strategic dependency

(420) The Commission acknowledges IPCEI ME/CT's furthering of the Union's policy to decrease a clearly identified, significant and strategic dependency on non-European microelectronics products and components (see recital (387)). This is consistent with point 21(g) of the IPCEI Communication.

(421) In view of all of the foregoing, the Commission considers that on grounds of section 3.2.2 of the IPCEI Communication, five out of seven general positive indicators, in accordance with point 21 of the IPCEI Communication are met.

(c) Specific criteria

Specific criteria for projects involving R&D&I and FID activities

(422) All individual projects within the four WS comprise either R&D&I or FID activities, or both.

(423) Point 22 of the IPCEI Communication provides that R&D&I projects must be of a major innovative nature or constitute an important added value in terms of R&D&I in light of the state-of-the-art in the sector concerned. According to point 23 of the IPCEI Communication, projects comprising of FID must allow for the development of a new product or service with high research and innovation content or the deployment of a fundamentally innovative production process. Regular upgrades without an innovative dimension of existing facilities and the development of newer versions of existing products do not qualify as FID.

(424) Further, point 24 of the IPCEI Communication defines FID as the upscaling of pilot facilities, demonstration plants or of the first-in-kind equipment and facilities covering the steps subsequent to the pilot line including the testing phase and bringing batch production to scale, but no mass production or commercial activities.

(425) In general, the Commission verified at the level of individual aid beneficiaries and per project within the different WS that each aid beneficiary has a well-defined and documented research programme regarding the innovations brought forward. The Commission conducted a technical assessment of each individual project to determine whether the projects that contain R&D&I and FID activities comply with the innovativeness requirements as laid out in the IPCEI Communication. Individual projects were deemed to have shown innovation, if they could demonstrate at least one of the following general advances that are relevant for both R&D&I and FID:

- technical performance beyond that of the current state-of-the-art technology at global scale;
- deployment of a technology at a scale that clearly goes well beyond the current state-of-the-art at global scale; and
- innovative applications or innovativeness of overall processes / approaches.

(426) In particular, the innovative nature of each individual project carrying out R&D&I and FID activities was analysed taking into account the following specific principles and parameters.

(427) For the R&D&I:

- state-of-the-art: the Commission has compared all product and process innovations of each participating undertaking against the state-of-the-art on the market at global scale;

- innovation: as regards the technical assessment of the innovative nature of the different projects, the Commission examined whether each individual project set specific targets for achieving the innovation required for the R&D&I activities proposed; whether those activities and targets go beyond the state-of-the-art; the innovations brought forward; and the benefits and expected results stemming from these innovations; and

- technical process/approach: the participating undertakings were asked to provide a clear description of the technical process/approach needed to reach the innovation targets. The Commission assessed in this context the type of technology used, the challenges encountered by each participating undertaking (see section 2.2.2.2) and the means chosen to overcome those challenges.

(428) For the FID:

- the Member States described the testing, sampling and upscaling processes implemented by each participating undertaking during the FID and explained how they differed from mass production and normal commercial activities. The Commission examined whether the FID contains important R&D&I activities for example the optimisation of innovations developed in the R&D&I phase, the deployment and integration of technological innovations in industrial settings and production processes and the scaling up of different technology and processes from pilot to industrial scale; and

- the Commission further assessed the duration of the FID of each individual project, and whether each participating undertaking provided meaningful KPIs and evidence of the FID duration, notably the criteria determining its start (i.e., at which point the undertaking starts using its pilot and industrial lines) and end period (i.e., at which point the undertaking produces samples, as well as the liability and return conditions applying to feedback sales and sales during the FID) and the scale of the FID to mass production (e.g., whether the FID envisaged by the individual projects is disproportionate in terms of size in comparison to the number of samples and tests projected).

(429) Based on the information provided by the notifying Member States and following an assessment against the relevant factors listed above, the Commission considers that the R&D&I and FID activities carried out in all of the four WS aim to advance the relevant technology substantially beyond the current state-of-the-art. The main general innovations and key expected results that the Commission identified as part of its assessment are described in the following recitals.

(430) The Commission considers that the Member States have demonstrated the innovativeness of all the individual projects within the four WS, including both

R&D&I and FID activities, in all areas of the microelectronics and communication technologies value chain that are specifically targeted by IPCEI ME/CT.

Major innovative nature and expected results

(431) The Commission considers that the Member States have demonstrated the innovativeness of IPCEI ME/CT including both R&D&I and FID activities, in all areas of the microelectronic and communication technologies value chain that are specifically targeted by IPCEI ME/CT.

(432) In WS-SENSE, the focus will be on the development of scalable sensor technologies and processes for the collection and digitalisation of data in multiple application fields. The main innovative actions envisaged by the participating undertakings in all of the WP mentioned (see recitals (67) to (70)) in order to overcome the challenges faced in the WS (see recitals (27) and (28)), consist of the following:

- developing 2D material technology and manufacturing processes for use in advanced sensor technologies;
- installing new tools for pilot line manufacturing of high volume 2D material technologies;
- developing and validating process integration of eco-friendly materials for new innovative smart sensors;
- processing integration of new substrates, material layers and masks;
- emerging material systems and advanced thin film deposition technologies;
- exploring and developing equipment for process, characterisation, and metrology inspection;
- developing compound semiconductor processes, advanced heterogeneous packaging techniques and wafer level integration;
- designing components and modules with sensitivity, speed, pixel pitch, format and functionality performances going beyond current state-of-the-art;
- developing high integration of electronics and mechanics with biology and bio-inspired MEMS devices;
- validating in manufacturing lines new innovative equipment for eco-friendly smart sensors;
- developing advanced manufacturing technologies on 100mm, 200mm and 300 mm wafer size for emerging MEMS and sensor devices;
- developing methods and technologies to analyse durability, repairability, reliability and long-term performance of thin films at wafer level scale;
- deploying of multilayer optical sensors for integration, near infrared (“NIR”) and IR sensors, and laser engines for LiDAR;

- wafer level integration of MEMS and microfluid structures and vertical integration of CMOS and More-than-Moore platforms.

- integrating glass-related materials in microfluid systems and pilot manufacturing of scalable MEMS sensing systems for biological applications.

- designing and implementing methodologies for testing the robustness and resilience of sensors, chips, wafers and microelectronic elements in harsh environment (in terms of radiation, vibrations and temperature);

- building new testing labs for complex testing of radiation tolerant sensors;

- streamlining the process of assembling and optimising components, while applying constraints through multi-domains (i.e., chip, package and board) and multi-physics (i.e., thermal, optical, electrical and mechanical) design processes;

- developing advanced packaging and heterogeneous integration technology for microelectronic, optoelectronic and microfluidic systems;

- packaging sensor devices in large volumes to meet market demands;

- developing new substrates and interposers to co-package sensor, microfluid and electronic devises in compact sub-systems;

- optimising assembly concepts for photonic integration, including optical alignment relaxation concepts for passive alignment processes;

- deploying new assembly processes between components and waveguides on substrates and in-boards;

- adapting testing technologies for integrated sensors;

- designing of IP for ultra-low-power systems on chip ("SoC"), AI algorithms and edge-computing;

- innovative design and architectures for the next generation of sensors, including UWB, radar and infrared ("IR") sensors;

- implementing AI algorithms for process control, device quality improvement and decision-making support;

- advanced prototyping and sampling, qualification for ramp-up and for industrialisation of sensors, components and modules;

- designing, developing and prototyping advanced sensor-based systems for mobility applications, such as automated driving, and for isolating biomarkers in organic samples;

- developing and prototyping advanced automotive (sub-) system and validation solutions based on novel sensor technologies, advanced electronics, signal processing and embedded AI software;

- designing and implementing tools for AI modules for various chipset architectures;
- developing MEMS, glass-related materials, sensor/sample interfaces, AI, low-power MCU and high energy photon sensors;
- pilot manufacturing of advanced sensor-based (sub-) systems for mobility applications;
- pilot manufacturing of advanced automotive (sub-) system and validation solutions based on novel sensor technologies, advanced electronics, signal processing and embedded AI software; and
- embedding AI modules to a set of smart grid sensors/actors, notably smart meters, EV chargers, energy gateways and testing.

(433) The key expected results of R&D&I and FID activities and the corresponding contributions of the participating undertakings in the respective WP of the WS-SENSE are the following:

| Expected results | Participating undertakings |
|---|---|
| **Materials:** develop, apply and test ultra-high-performance thin-film materials such as: 2D, organic, III-V, II-VI, magnetic, piezoelectric, and ferroelectric materials for sensing technologies. This will also include the development, application and testing of tailored and functional semiconductor substrates for material and energy reduction of sensor devices. In addition, it is needed to evolve towards cost-effectively manufacturing of 2D materials at high volumes. | Lynred, MEMC, Wacker |
| **Tools & Equipment:** integrate new tools and equipment for handling, processing, characterisation, metrology and inspection of new materials, new processes, new packaging, sensing chips and wafers for the manufacturing of sensing devices. | Thermo Fisher, Lynred |
| **Advanced thin film technology, new sensor technologies and smart manufacturing:** create high/small volume processing/manufacturing platforms for emerging thin-film and MEMS products based on 200/300 mm, and develop small volume processing technologies on very specific materials for specialised sensing devices, including the implementation of AI-planned, steered and controlled large compound semiconductor devices. | ADI, Bosch-DE, Elmos, Lynred, IFX-DE, Osram, STM-FR, STM-IT, Vigo, X-FAB-FR, X-FAB-DE |
| **Heterogeneous integration & assembly and packaging technology:** implement advanced high-reliability packaging, including panel and wafer level packaging for heterogeneous integration of ASIC, ASPIC and sensor dies, as well as passive devices. Improve the integration and packaging of compound semiconductors (including III-V, II-VI, InP photonics and quantum photonics) and Si, replacing flip-chip technology in order to make it economically viable. | Bosch-DE, Continental-RO, Elmos, GF, IFX-DE, Lynred, Osram, STM-FR, STM-IT, Trumpf Photonic, Vigo, X-FAB-DE |
| **Advanced testing for integrated sensors:** develop and integrate new characterisation and test procedures, including for multi-die optical sensors, automotive-quality ADAS-related sensors, space sensors, analog sensors on wafer (both electronic and photonic) and final part level. Furthermore, develop new methodologies and tools for standardised testing of new types of materials and sensor applications under normal and extreme operating conditions (e.g., | Continental-RO, Elmos, Lynred, Vigo |

| | |
|---|---|
| temperature, pressure, humidity, chemical aggressiveness, dust, or radiation). | |
| **Ultra-low energy sensors for industrial, mobile and IoT applications and sensors for enabling energy efficient systems:** develop smart components with high level of integration of multi-sensors and IC for data-analytics and edge-computing, including hybrid and optical/microwave/analog/digital approaches. | Bosch-DE, FMC, Lynred, NXP-AT, Obducat, Osram, STM-FR, STM-IT, Trumpf Photonic, Vigo, X-FAB-FR, Infineon-DE |
| **Sensors for environmental protection and food safety:** develop miniaturised, efficient and integration-capable compound semiconductor components for detection and emission. | IFX-DE, Lynred, Osram, STM-IT, Vigo |
| **Sensors for automotive mobility solutions and perception components:** develop advanced perception components, both active as well as passive components, with ML features, including radar, lidar, UWB, imaging, near- and mid-infrared, and ultrasonic sensors. | ADI, AVL, Bosch-DE, Bosch-RO, Continental-RO, Elmos, FMC, IFX-DE, Lynred, NXP-DE, NXP-NL, NXP-RO, Osram, STM-FR, STM-IT, Trumpf Photonic, Vigo, X-FAB-FR |
| **MEMS and special components for a safe and secure digital life and health:** develop high-performance MEMS sensors, MEMS above IC sensors, quantum-sensors, bio-inspired MEMS and Si-based micro-fluidic MEMS. Also, develop highly sensitive biomedical, chemical and biological sensors with molecular recognition and different electrical approaches, and sensors with improved robustness and/or easier manufacturable for harsh environments, including radiation-tolerant environments (e.g., space or medical) and automotive qualification. | ADI, Lynred, Menarini, Osram, STM-IT, Vigo, X-FAB-DE |
| **Automotive sensing systems, system integration and validation:** develop and pilot-manufacture innovative measurement, validation and monitoring solutions based on newly integrated advanced sensor technologies, software and simulation for the development, testing, monitoring and validation of automotive sensors, components and systems on testbed, on-board and on-road (e.g., for electrification (battery EV/fuel cell EV), ADAS/AD and future remote (exhaust/non-exhaust) measurement). | AVL, Bosch-DE, Bosch-RO, Continental-RO, Elmos, Mycroft, NXP-RO, Vigo |
| **Health sensing systems and specific system features:** develop and pilot-manufacture advanced sensing systems for biological applications (lab-on-chip). | Menarini, STM-IT |
| **Health specific system features**: develop and pilot advanced low-power edge-AI matching low computing power requirements for sensors MCU. Also, ensure multi-radio non-interferences for wireless systems including secured AI/ML functionalities and create the ability to package and test sensor-waveguide-laser systems in large volumes and short time. | AVL, Bosch-DE, Bosch-RO, Continental-RO, Elmos, Mycroft, NXP-RO, STM-FR, Vigo |

***Table 24: Expected results from innovation - WS-SENSE***

(434) WS-THINK will focus on the energy efficient and secure data processing and storage at all levels of the microelectronics and communication technologies value chain. The main innovative actions envisaged by the participating undertakings in all of the WP mentioned (see recitals (100) to (103)) in order to overcome the challenges faced in the WS (see recitals (32) and (33)), consist of the following:

- developing advanced Si substrates, including FD-SOI that are expected to enable energy-efficient components down to 10 nm, supporting thus the green and digital transition;

- developing 2D materials (e.g., graphene and transition metal dichalcogenides) for semiconductor applications enabling further transistor shrinkage and novel

photonic technology and applications, such as the integration of photonic circuits in the backend of electronics;

- developing 2D materials tools and processes for high volume manufacturing ("HVM"), enabling the integration into several semiconductor applications;

- developing new disruptive EDA tools for new processor designs that are expected to reduce time to market, risks, costs and design errors, while increasing performances, energy efficiency, chips per wafer, thereby decreasing the impact on the environment;

- developing EUV lithography system though the design of high-NA EUV lithography scanners, and the integration of several technologies, namely quality optical components and modules, advanced high-power lasers for EUV light source, mask process capabilities, mask repair tool, and advanced metrology and inspection tooling in order to increase yield, reduce waste and improve sustainability;

- developing innovative 3D structural and dimensional metrology tools and processes with higher precision and throughput to meet the requirements set by the next decade semiconductor manufacturing roadmaps;

- developing wafer level packaging processes with complex single die, flip chip or chiplet integration within all semiconductor packages for secure flash memory and IoT, based on embedded multi chip packages ("eMCP") or SiP technologies;

- usage of emerging memories embedding intelligence into sensor new solutions for smart BMS;

- developing next generation ferroelectric memory on advanced technology nodes;

- driving the innovation on existing digital or embedded non-volatile memory technology platforms by providing extensions in functionality towards high frequency operation, efficient power drivers, energy efficiency, IoT, AI, and new architectures and methods for data centres;

- scaling-up and combining of chips in advanced packaging ("AP") and panel level packaging ("PLP"), and contactless testing;

- creating beyond state-of-the-art technology platforms for low-power computing design, including differentiated technologies, enabling embedded memory, low-power components and secure elements;

- developing system integration by combining electronics components which cannot be integrated monolithically in one technology;

- developing associated back-end technologies, such as substrates for advanced packaging, which aim at revealing the full performance at system level, by combining the shortest pathways thanks to miniaturized interconnections, while keeping the power supply stable and the data transfer rate extremely high;

- heterogeneous package integration by combining passives (i.e., power and sensor) components with active (i.e., CMOS, III/V, GaN, SiC) components to yield optimum performance in terms of power consumption and functionality;

- developing IoT technology and AI techniques for test, inspection, quality analysis, advanced scheduling and predictive maintenance;

- innovative IP, SOC, SiP and processors along the following major axes: general purpose computing, HPC and AI specific computing, automotive computing, security, power and BMS and novel memory and packaging;

- developing open RISC-V architecture to allow the participating undertakings to customise their chips both at the instruction and at the microarchitecture levels, thereby optimising performance, power and cost;

- mixing new generation technologies with the use of heterogeneous architectures or domain specific accelerators, thereby creating new solutions for downstream market demands;

- developing novel post-quantum cryptography solutions that are expected to increase security in all downstream markets, with a particular focus in the automotive market;

- developing novel microarchitectures with AI/ML extensions to support CPU, GPU, TPU, fuzzy logic, FPGA and neuromorphic capabilities;

- developing technology components and design blocks for battery management IP and chips, including chip integration of BMS;

- developing methods for design space exploration and early system design and development (e.g., applying system engineering practice for component-based architecture design for scalable system; system packaging linked to component dissipation constraints and compatible with environmental condition for electromagnetic compatibility and tightness; use of digital twins for system evaluation by simulation/emulation etc.);

- integrating technology capable to make assembly and testing of low pitch components and enhancing the assembly steps by making use of new machinery process; and

- integrating AI/ML for improving product quality and supporting the safe and secure IT infrastructure to control and administer manufacturing and delivery with logistic and billing services.

(435) The key expected results of R&D&I and FID activities and the corresponding contributions of the participating undertakings in the respective WP of the WS-THINK are the following:

| Expected results | Participating undertakings |
|---|---|
| **Advanced materials including substrates, gases, masks etc. for new technology generations:** develop new bulk 300 mm Si and FD-SOI substrate generation, with improved flatness, metal contamination levels and adapted resistivity and with active Si layer and buried oxide thickness uniformity for FD-SOI substrates. Furthermore, develop the next level of polysilicon ready for leading edge-(2nm) applications, and integrate 2D materials in an advanced node for photonics applications up to a production line. Also, develop and implement mask manufacturing line with advanced performances. | MEMC, Soitec, Wacker |
| **EDA tools and modelling:** develop new advanced gap-filling general purpose processor EDA design tool/methodology and tools that enable the effective design of high-performance processors for heterogeneous computing. Also, develop high-density (down to 3nm) 2.5D/3D IC architectures operating at high frequency (2GHz to multiple 100s GHZ), as well as tools for developing FPGA, taking into account power issues. | Codasip |
| **Equipment for new technology generation:** develop and test, for high-NA EUV lithography, the techniques towards 1nm (e.g., 10 angstroms/A10) lithography and below. This encompasses extensions/upgrades for the roadmap, from 1.4nm up to 0.7nm for the lithography tool, development of high-NA EUV lithography optics systems capable for technology nodes at 1 nm, and tools for EUV photomask repair, inspection, metrology, and source illumination technology. Also, develop advanced tools for 2D material supply, increase, for metrology equipment, the speed of the workflow through digitisation of the manufacturing equipment value chain using for instance digital twinning and AI, develop 3D full die (“3DFD”) in-line metrology and inspection system for advanced node (< 7nm) semiconductor manufacturing, and develop and test software for AI/ML computational models to enhance accuracy, resolution, and speed of microscopy and scatterometry measurements. For Assembly equipment and test, develop contactless test and review systems for AP and PLP applications, and develop a fully trusted supply chain for back-end manufacturing of eMCP and SIP products in secure flash memory and IoT devices. | ASML, Bizzcom, BLK, Nearfiled, Thermo Fischer, Zeiss |
| **Front-end technology platforms:** develop new generations of FD-SOI technology (platform and selected extensions); develop new capabilities on charge based embedded memory technology platforms; create and exercise complete technology design platforms based on engineering, procurement and construction management (“ePCM”), the most suitable non-volatile memory technology for in memory computing (“IMC”); develop intelligent integrated power and sensor systems, and perform technology enablement for new microcontroller and system architecture to embed | GF, Elmos, FMC, IFX-DE, STM - FR, STM-IT, X-FAB-FR |

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| intelligence into sensors and actuators; develop AI-enabled, secure and connected predictive maintenance technologies for increased productivity of equipment manufacturing tools in fab metrology labs for ramp-up and production; regarding emerging techniques and platforms, develop new ferroelectric memory technology on advanced technology nodes, integrate 2D materials in advanced nodes, and develop advanced tools for 2D material supply. | |
| **Back-end technology platforms (packaging):** develop an IC-substrate based technology platform enabling high data transfer rates in ultra-dense packages; design, build and ramp- up a prototype and production fab for IC-substrates; create advanced and high quality packaging technology for high-end microcontrollers, targeting ADAS automotive application; set-up flip-chip on organic substrate assembly and test line up to lower nodes for both low and medium volumes; develop ultra-thin low parasitic capacitive technologies; integrate and demonstrate LSC/DSC decoupling; develop processes and integration concepts for heterogeneous chip integration in package; and, develop a BMS IC design fabrication and assembly platform. | AT&S, BLK, Elmos, GF, STM-MT, Sunlight, Teledyne |
| **Manufacturing sciences and digital transformation:** develop and introduce smart manufacturing methodologies, that is the introduction of big data supported AI in manufacturing and manufacturing control, notably smart factory, Industry 4.0 and AI/ML. | AT&S, Elmos, GF, STM-FR, STM-MT |
| **General purpose IP and chips:** develop a collection of novel reusable IP for spanning the spectrum of computing requirements from low-power microcontrollers to high-performance processors; design and implement RISC-V industrial set architecture based processors; integrate CMOS and other technologies, notably embedded NVM technologies, IoT, dedicated interfaces, providing a rich set of features targeting multiple application domains, such as edge-AI, IoT, HPC etc. | Codasip, STM-FR, STM-IT, Tachyum |
| **AI and HPC IP and chips:** develop next generation FPGA and AI accelerators based on innovative architecture; develop a complete SOC and associated peripheral component interconnect express (“PCIe”) board targeting HPC and/or workloads from edge to the data center; realisation of a toolbox to enable embedding intelligence for new embedded processing technologies and components related to data processing and data storage at all levels, with AI through ePCM based and neuromorphic architectures; develop memristor-based components and modules along the entire value chain and design of data converters (i.e., ADC and DAC) chips; incorporating ISA extensions for AI/ML and security solutions, in order to leverage the RISC-V industrial set architecture, processors and IP for suitable low-power AI and HPC; and, develop high-performance, energy efficient and/or secure SoC devices and SiP modules mounted on a PCB accelerator card for | Cologne Chip, Continium, Openchip, Semidynamics, STM-IT |

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|---|---|
| HPC, AL/ML/DL applications and from the edge to research and enterprise centers and systems. | |
| **Automotive and secure IP and chips:** develop advanced SoC for future vehicle E/E and architectures; develop an automotive grade processor […] for future vehicle architectures with ultra-low-power consumption and high processing capabilities; develop secure and safe software stacks for highly integrated multi-core multi-processor architecture and multi-connectivity devices; develop radar transceivers with optimized RF for ADAS systems; and, develop a post quantum secured processor architecture and platform (RISC-V based). | Elmos, NXP-AT, NXP-DE, NXP-RO, Bosch-DE, Bosch-RO, STM-FR, STM-IT |
| **Power and battery management IP and chips:** develop a complete battery-less MCU, selected IPs for intelligent, safe, and secure BMS, and a BMS IC design fabrication and assembly platform. | Continium, NXP-AT, Sunlight, X-FAB-FR |
| **Novel memory chips and technologies:** develop new ferroelectric memory technology on advanced technology nodes, and radically new chip concepts, connecting with and integrate in processors and sensors, to achieve future needs of low-power, high cycling stability, high-speed and data retention properties. | FMC |
| **System design and development (including board design, assembly and testing):** development of technology building blocks for E/E architecture and vehicle computer; development of modular, scalable, and upgradeable electric/electronic architecture for vehicle lineup, of a physical safety system, through AI, 5G/6G communication systems whose data will be protected by security algorithms; development of high-performance, energy efficient and secure accelerator modules for HPC, AL/ML, DL applications, from the edge to research and enterprise centers and systems; and, development of the printed board assembly and co-integration for the next generation of BMS. | Bosch-DE, Bosch-RO, Continental-FR, Elpos, Openchip, Sunlight, Tachyum |
| **Software and visualization techniques (including digital twins):** develop software and virtualization techniques to support HPC, especially, RISC-V based solutions. This also includes the demonstration of HW/SW codesign for many domains, including processors and accelerators, intelligent motor control, and the design of a scalable and upgradeable E/E architecture using system engineering thinking. | Continental-FR, Elmos, Mycroft, Openchip |
| **Component driven architecture:** develop building blocks for vehicle computer and controller, identify and explore solutions for the accelerators and processor Prodigy2 for downstream industries (e.g., HPC, cloud, telco 5G, edge-AI, embedded AI, smart manufacturing, space etc). | Continental-FR, Mycroft, NXP-RO |

***Table 25: Expected results from innovation - WS-THINK***

(436) WS-ACT will focus on the development and implementation of technologies aiming at how to treat the information collected and processed in the WS-SENSE and WS-THINK. The main innovative actions envisaged by the participating undertakings in all of the WP mentioned (see recitals (141) to (144)) in order to overcome the challenges faced in the WS (see recitals (37) and (38)), consist of the following:

- developing more advanced and efficient power electronics, with higher operating voltages, lower power dissipation and higher switching frequency for multiple applications, notably energy generation and storage from renewable sources, smart grids, mobility, data centres, 5G base-stations, AI, IoT and industrial equipment;

- developing WBG semiconductors, such as SiC or GaN, which have a larger bandgap than Si semiconductors, thereby leading to a higher breakdown voltage, less switching and conductive losses, resulting to lower energy losses and higher device efficiency. In addition, the WBG semiconductors have a higher frequency capability, which reduces the number of passive components, and, thanks to their better temperature resistance, they have decreased cooling requirements, thereby enabling reduced system volume and easier packaging;

- designing Si based technologies for the development of power applications, where wide bandgap materials are not best suited, notably for IGBT devices, ultrathin MOSFET and 40nm BCD;

- developing a higher level of integration of components to meet the requirements of heterogenous downstream applications, and also a higher modularity/scalability from discrete components to generic modules, with the purpose of enabling the development of compound semiconductors. The latter, such as GaN, SiC and GaAs are expected to further push the monolithic integration solutions for faster design cycle;

- development of new module and package concepts, and package prototypes with optimised switching behaviour and enhanced thermal/electrical performance

- developing materials and substrates with larger diameter to improve Si and compound semiconductor crystal growth and epitaxy equipment, thereby enabling higher quality products, able to function at high voltages without compromising the conduction behaviour;

- developing both the Si smart-power (e.g., high-density will integrate more and more complex and diversified functions on the same chip and guarantee high quality and reliability in all types of application environments) and discrete-power products (e.g., super junction high-voltage transistors, etc.);

- concerning SiC technology, developing materials (e.g., wafers and wafer diameter, epitaxy, heteroepitaxy, etc.), and realising the CMOS technology from the point of view of basic technological steps, such as oxidation, annealing, ion implantation, metallization, etc;

- developing micro-LED technology, which presents major advantages in terms of contrast, colour gamut, brightness and latency for display applications, such as smart watches, cell phones, headsets and large screens;

- concerning WBG transistors, developing new components/modules combined with state-of-the-art technology within PCB, as well as novel control functions to enable the smart usage of high frequencies commutations afforded by the wide bandgap transistors;

- implementing and driving electronic components, such as PCB and all the associated functionalities related to the electronic system, such as transformers or interconnections between PCB and components, as well as control functions, to enable higher voltages and broader usages;

- developing mechatronic integration aiming at enabling the electronic system to operate within the application product, thanks to mechanical interfaces, housing and thermal management, taking into account specific constraints and operating conditions;

- developing new efficient energy harvesting solutions based on new compound semiconductor materials.

- using advanced Industry 4.0, with the aim at achieving the industrial footprint required for the targeted volume, reliability and quality; and

- developing new validation and monitoring solutions, including thermal conditioning systems for high-performance dyno converters/inverters.

(437) The key expected results of R&D&I and FID activities and the corresponding contributions of the participating undertakings in the respective WP of the WS-ACT are the following:

| Expected results | Participating undertakings |
|---|---|
| **Simulation tools and semiconductor equipment:** to develop new modelling and simulation software to facilitate high efficiency design, EMC and manufacturing processes for power electronics based on Si, wide bandgap and novel materials, reducing product's time-to-market and the testing effort. Furthermore, to develop new improved Si, wide bandgap and novel materials equipment, notably graphite based SiC, GaN, GaAs semiconductor crystal growth, ion implantation and epitaxy equipment. | mi2, SGL |
| **Materials and substrates:** to develop advanced materialS for beyond state-of-the-art Si power, wide bandgap (i.e., SiC and GaN) and advanced GaAs with different wafer substrate diameters (100mm, 150mm, 200 mm and 300 mm). | Aledia, EEMCO, FCM, IFX-DE, MEMC, SGL, Soitec, STM-FR, STM-IT, ZF |
| **Manufacturing science and quality:** to develop and introduce smart manufacturing concepts and the implementation of efficient smart Industry 4.0/5.0 in production systems (e.g., automation solutions, Industrial IoT, big data acquisition and analysis, AI/ML/DL for energy efficiency and tool usage, data acquisition, predictive maintenance, process monitoring etc.). | ADI, Aledia, Bosch-DE, EEMCO, FCM, IFX-AT, IFX-DE, STM-FR, STM-IT, X-FAB-FR, ZF |
| **Si based technologies**: to develop new low ohmic | Bosch-DE, GF, IFX-AT, IFX-DE, |

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|---|---|
| 300 mm substrate material, complex integration BCD technologies (300mm and 200 mm), advanced MOSFET and IGBT concepts, with ultrathin wafers manufacturing. | Semikron-DE, STM-FR, STM-IT, X-FAB-FR |
| **Technologies based on wide bandgap and other new materials (e.g., advanced GaAs):** to develop wide bandgap, and GaAs processes prototyping proved in 150 mm and 200 mm pilot lines. | Aledia, Bosch-DE, IFX-AT, mi2, STM0FR, STM-IT, ZF |
| **Actuation and harvesting technologies**: to develop actuation manufacturing technologies, especially for MEMS devices, addressing industrial results for 200 mm and 300 mm MEMS manufacturing processes. | Bosch-DE, GF, STM-IT |
| **Power Si and Smart Power devices:** to design and develop trustworthy power devices of high quality and efficiency (e.g., BCD and vertical intelligent power ("VIPower") products, power discrete based on Si etc.), reducing die size and cost of future products, while improving performances, robustness, functional safety, integration and total cost of ownership. | ADI, Bosch-DE, Continental-RO, Semikron-SK, STM-FR, STM-IT |
| **Power SiC and GaN components:** to develop wide bandgap and other material components, based on, for instance, new wafer diameter technology and new IC configurations, enabling the WBG heterogeneous integration for higher performances, volumetric reduction and energy efficiency. | Bosch-DE, Continental-RO, Semikron-SK, STM-FR, STM-IT, ZF |
| **Power packaging and modules:** to develop package prototypes, including PLP and heterogeneous integration technology (e.g., new generation power modules with optimised switching behavior, new module and package concepts (e.g., dual-side cooling) to enhance thermal/electrical performance for high-power modules for vehicle electrification etc.). | IFX-DE, Semikron-DE, Semikron-SK, STM-FR, STM-IT, Valeo, ZF |
| **Actuators and micro-LED:** as regards the actuators, to develop emerging MEMS actuation technologies and components (including micro and nanofabrication processes and tool and equipment optimisation), in order to demonstrate tnew solutions for machine-to-machine interaction, human machine interface and human computer interaction (e.g., ultrasonic piezo devices ("pMUTs"), laser and optics and power supply combines in miniature modules etc.). For micro-LED, to develop new components and modules for power efficient displays and projector technologies (e.g., actuated micro-mirrors, CMOS with new efficient display architecture etc.) | Aledia, Bosch-DE, Bosch-RO, Continental-RO, STM-IT, X-FAB-FR |
| **Energy efficiency and harvesting:** to develop new efficient harvesting solutions (e.g., high efficiency optical power converters based on advanced GaAs, integrated smart actuators for EV etc.) for applications based on the use of remote and autonomous sensing and actuation devices. | ADI, Bosch-RO, Continental-RO, STM-IT |
| **PCB:** to develop new electronic PCB and associated control functions (e.g., concepts of wide bandgap PCB for automotive high voltage converters, with | Continental-FR, Renault, Valeo, Vitesco, ZF |

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| advanced switching control addressing high voltage power electronic systems etc.), in order to implement new components/modules and, for instance, enable the smart usage of high frequencies commutations of wide bandgap transistors. | |
| **Power electronic blocks:** to perform a smart system integration of the electronic components (e.g., PCB) and all the associated functions of the electronic system (e.g., transformers, capacitors, filters etc.), enabling the integration of PCB with the wide bandgap technologies for the related functions of power electronic blocks (e.g., chargers, converters, inverters or heaters). | Continental-FR, Renault, Valeo, Vitesco, ZF |
| **Power electronics/actuator systems:** to develop the integration and validation of mechatronic power electronics (sub-) systems using Si- and/or wide bandgap and novel technologies, such as thermal conditioning of electronic components, that can be easily integrated into downstream applications (e.g., electric powertrain) or testing equipment (e.g., control benches). | AVL, Continental-FR, Renault, Valeo, Vitesco, ZF |

***Table 26: Expected results from innovation - WS-ACT***

(438) WS-COMMUNICATE will focus on the development of technologies and communication infrastructure aiming at receiving from and transmitting to electronic equipment the information collected and processed in the previous WS. The main innovative actions envisaged by the participating undertakings in all of the WP mentioned (see recitals (174) to (177) ) in order to overcome the challenges faced in the WS (see recitals (42) to (44)), consist of the following:

- developing connectivity technologies that can have 10 to 100 times more performance while at same time being more energy efficient, as compared to current connectivity solutions
- developing adequate EDA tools to improve electromagnetic crosstalk analysis for advanced node and high-frequency chip and the model of next generation Wi-Fi systems, as well as to speed up the design of novel domain-specific processor architectures with memory subsystems for achieving ultra-low-power consumption;
- developing advanced materials for RF serving new, diverse applications and requiring increase in frequencies, while reducing energy consumption;
- developing process technologies, such as GaN-on-SiC, which combines the high-power density of GaN with the high thermal conductivity and reduced RF losses of SiC, GaN-on-Si and GaN-on-SOI, in order to meet the requirements of the emerging 5G technologies that require dedicated RF front-end chipsets;
- implementing process modules and developing integration systems of the various individual process modules to one technology, carrying out device and technology optimisation after characterisation and simulation, to reach performance and reliability targets, developing and implementing measurement and validation techniques (for both performance and reliability) and automatic tools for data acquisition and process monitoring in the wafer fab;

- developing new photonic processes and components, which aim at optical communications and innovative optoelectronic chipsets, assembled in new developed robust and low-cost optical packages, thereby enabling high-speed interconnections among chipsets and elimination of electromagnetic interferences to communications;

- developing CMOS technologies for improved performance and power consumption to meet next generation wireless system semiconductor requirements;

- designing and developing new SoC for application in optical and radio communication systems;

- designing and validating algorithms, IP blocks, and SoC solutions for application in 5G/6G, and WiFi7, including ultra-low-power 5G/6G IoT modules, thereby maximising chip performance, while minimising chip power dissipation, process complexity and cost;

- developing different system architectures (e.g., classic RAN, cloud RAN, O-RAN etc.) for mobile communication systems (i.e., 5G/6G with edge-cloud AI and the supporting wireless and optical network transport), and IoT solutions, aiming at improving the performance of the chipsets implementing these communication systems;

- Developing chip and system design to guarantee secure hardware and secure connections at all levels of the microelectronics and communication technologies value chain; and

- developing all computing in-memory solutions which are crucial for designing and producing reliable industrial IoT ecosystems.

(439) The key expected results of R&D&I and FID activities and the corresponding contributions of the participating undertakings in the respective WP of the WS-COMMUNICATE are the following:

| Expected results | Participating undertakings |
|---|---|
| **EDA tools:** to focus on automation of the design: AI/ML extensions, such as RISC-V vectors, RISC-V extensions, or security RISC-V model functions. | Codasip |
| **Test and measurement tools:** to design and validate conducted RF and over-the-air ("OTA") RF test and measurement systems for new frequency bands. | R&S |
| **Substrates**: develop advanced materials (e.g., high-performance 150mm and 200mm diameter engineered substrates) for RF supporting new 5G/6G specs, and photonics, enabling increased optical link transmission rates and going beyond current bandwidths. | FCM, MEMC, Soitec, Wacker |
| **Polysilicon:** to develop chemicals of high purity and design novel processes and equipment, in order to reach specific resistivities for wafer devices that are required in 5G/6G applications on Si wafer substrates. | MEMC, Soitec, Wacker |

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| **Photonics technology:** to develop photonics building blocks and integration schemes for improving hybrid integration between the different photonic platforms and between photonics and electronic platforms, improving the functionality, performance, and applicability of the individual photonics elements, establish a stable and scalable footprint required for successful scale-up of the industrial capability on III-V, silicon nitride ("SiN"), lithium niobate on insulator ("LNOI") and Si photonics, and deploy demonstration of pilot runs of advanced photonic components. | ADVA, GF, STM-FR, Trumpf Photonic, X-FAB-DE, X-FAB-FR |
| **GaN and other III-V related RF technologies**: to specify and develop the GaN wafer material (e.g., substrates/epitaxial wafer) that will be deployed in RF GaN-on-SiC, GaN-on-Si and GaN-on-SOI technologies. This includes the implementation of suitable process modules in the corresponding manufacturing line, integration of various individual process modules to one GaN-technology, device optimisation after characterisation and simulation, technology optimization to achieve performance and reliability targets, development and implementation of measurement and validation techniques, modelling methodologies for devices leading to design kits, development, and implantation of automatic tools for data acquisition and process monitoring in the wafer fab and qualification. | GF, IFX-DE, R&S, Soitec, STM-FR, STM-IT, UMS, X-FAB-DE, X-FAB-FR |
| **CMOS technology:** developing new generations of BiCMOS, RF-CMOS, RF-SOI, FD-SOI RF technologies in order to meet RF requirements for telecommunications, radar sensing and high/speed/data processing, while at the same time achieving improved performance and reduced power consumption to meet next generation wireless system semiconductor requirements. | GF, IFX-DE, NXP-NL, STM-FR,X-FAB-FR |
| **SAW technology:** to develop novel micro-acoustic filter concepts based on piezoelectric thin film substrate technology. | Soitec |
| **Packaging technology**: to design and develop sub-systems based on heterogeneous building blocks, integrate different semiconductor technologies, provide packaging solutions in 2.5D/3D and optical connectivity, enabling a chiplet ecosystem of smart designs and packaging processes used in modular SoC development. | ADVA, Ericsson, GF, IFX-DE, NXP-NL, STM-FR, X-FAB-DE |
| **Assembly and test:** to develop innovative automation equipment, measurement/characterisation techniques, and back-end assembly and test for optical components, specifically for photonic transceivers and co-packaged optics for datacom, automotive, defence and aerospace applications. | IFX-DE, IRVI, KDPOF, NXP-NL, STM-FR, X-FAB-DE |
| **Optical and digital signal processing SoCs:** to evaluation chiplet approach as opposed to monolithic ASIC; to identify benefits that would enable separated optimisation of different SoC functions; to design and | ADVA, KDPOF, Nokia-DE |

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| verify chiplets used in coherent optical transceivers; to develop next generation high-speed optical transceivers and co-packaged optics based on hybrid/heterogeneous photonic IC for telecom/datacom applications; and, to develop full integrated optical transceivers and analog programmable processors for different applications. | |
| **Radio and digital signal processing SoCs:** to evaluate chiplet approach as opposed to monolithic ASIC; to identify benefits enabled to separate optimisation of different SoC functions, […] CMOS technology; to design, layout and verify chiplets used in coherent optical transceivers including analog, digital and photonic technologies. | Ericsson, IRVI, Nokia-FI, NXP-DE, NXP-RO, SIAE, STM-IT |
| **AD/DA Converter:** to design new high-performance and very low-power consumption algorithms and architectures for high-speed data converters (i.e., ADC and DAC) applied in optical communication; to develop RF digital front-end chips together with broadband ADC/DAC digitisers for 5G/6G mmW beamforming MIMO systems […] and beyond to co-integrate complex SoC; and to develop information architectures and circuits to get low-power consumption systems for IoT. | ADVA, Continium, IRVI, KDPOF, Nokia-DE, NXP-DE, STM-IT |
| **Domain specific accelerator based on RISC-V and/or ARM:** to develop domain-specific, customizable RISC-V accelerator/DSP for radio communication with AI/ML extensions for 5G/6G, with improved and innovative memory subsystem for AI/ML; to design special engines as vector units for AI/ML applications with the optimised instruction set; to design SW libraries for accelerators with different AI and ML approaches, O-RAN, cloud-RAN support, security stack support, etc; and to integrate electronics and photonic FPGAS and SoCs for improved energy consumption. | Codasip, IRVI, Nokia-FI, NXP-DE, NXP-RO, STM-FR |
| **RF design and power amplifier:** to develop power-efficient, wideband RF microelectronics for application in 5G/6G and WiFi7 frequency bands, mm wave transport, as well as a smart virtual antenna for end-devices capable of addressing both terrestrial and non-terrestrial communication. | Ericsson, IFX-DE, IRVI, Nokia-DE, NXP-DE, NXP-NL, R&S, SIAE, STM-IT, STM-FR |
| **Cyber security and IoT:** to develop post-quantum cryptyography capabilities that include protection against external attacks; to develop new architectures for quantum-computer-safe edge-processing; to develop cyber protection and cyber defence technologies aiming at ensuring the total cyber security of 5G solutions using “Security by Design” process; to implement hardened security features in components used in pluggable coherent transceiver modules; to develop new smart power devices where the networking and connectivity will be the key function; to develop SIM security features for new environments such as board mounted near the engine | ADVA, IRVI, NXP-RO, STM-IT, STM-FR |

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| of a car or on a power meter; to develop short- and long-range, low-power wireless technologies for IoT that complement 6G communications technology, as well as deploy IoT-5G/6G modules with ultra-low-power consumption and IoT trials. | |
| **Optical subsystems:** to develop subsystems for optical communication applications that comprise highly integrated, advanced photonic, and electro-optical components, including transceivers that power high-capacity optical communication networks and switching and interconnection modules. | ADVA, KDPOF, Nokia-DE, STM-FR, Trumpf Photonis |
| **Radio subsystems:** to develop wireless transceivers for future radio systems in communication networks. | Cogninn, Nokia-DE, SIAE |
| **SW/HW co-design:** to develop, validate, prototype, and pilot manufacture eco-friendly and (cyber-) secure SW/HW, notably flexible transceiver, SW package on chips, platform for O-RAN and cloud-RAN, data acquisition and transmission, and solutions for IoT, automotive and satellite. | ADVA, Airbus, AVL, Cogninn, IRVI, Nokia-DE, NXP-RO |
| **E2E Critical Radio System Pilot:** to design, build and run end-to-end communication solutions network (i.e., terrestrial, radio, optical and satellite). | ADVA, Airbus, Cogninn, Nokia-DE, Orange, SIAE |
| **User terminals:** to provide reliable, smart, and secure end-user terminals as standalone devices and modular building blocks for device integration, notably in IoT and vehicles. | Airbus, Cogninn |
| **Edge-cloud and edge-AI solutions (RAN/IoT):** to develop edge-servers, acceleration solutions, AI/ML integrated with electronic and photonic HW, new monitoring and control solutions and end-to-end applications. | Airbus, AVL |

***Table 27: Expected results from innovation - WS-COMMUNICATE***

#### 3.3.2.3. Importance of IPCEI ME/CT

(440) According to section 3.3 of the IPCEI Communication, in order to qualify as an IPCEI, a project must be important quantitatively or qualitatively. As demonstrated below, IPCEI ME/CT is particularly large in size and scope and implies a very considerable level of technological and financial risk.

(441) The Commission considers IPCEI ME/CT to be an important project meeting the quantitative and qualitative requirements set out in section 3 of the IPCEI Communication, based on the following:

- IPCEI ME/CT represents an important contribution to Union's objectives (see recitals (362) to (371));
- IPCEI ME/CT is designed to overcome important market or systemic failures (see recitals (372) to (387));
- 14 Member States participate in IPCEI ME/CT (see recital (389));
- all Member States were given the opportunity to participate in IPCEI ME/CT (see recital (390));

- IPCEI ME/CT generates positive spillover effects (see recitals (391) to (401));
- IPCEI ME/CT involves important co-financing by the aid beneficiaries (see recital (402));
- IPCEI ME/CT complies with the principle of 'do no significant harm' (see recitals (403) to (414));
- The Commission was involved in the design of IPCEI ME/CT (see recital (415));
- The governance of IPCEI ME/CT involves the Commission (see recital (416));
- IPCEI ME/CT involves important collaborative interactions (see recitals (417) and (418));
- IPCEI ME/CT involves co-funding or co-financing from a Union fund (see recital (419)); and
- IPCEI ME/CT addresses a significant strategic dependency (see recital (420)).

(442) In addition, the Commission acknowledges the considerable level of technological, economic, financial and other risks for the individual projects within IPCEI ME/CT.

(443) Regarding the technological risks, the Commission notes that these may involve a failure in performance, cost and sustainability of the technologies developed in IPCEI ME/CT. To this end, unforeseen additional work (e.g., studies, modifications, tests, etc.) might become mandatory, thereby posing significant delays, which would inevitably result in additional costs to reach the initial objectives.

(444) In addition, the innovative solutions proposed by the participating undertakings may not be compatible with large-scale industrialisation or with the equipment available on the market, thereby resulting in delays in delivering the final innovative materials and advanced equipment. This is because of the lack of industrial-scale facilities producing the innovative building blocks along the entire microelectronics and communication technologies value chain. The difficulty, therefore, in producing innovative technologies is proportionate to the number of technical locks and challenges that need to be overcome, especially during FID, before introducing the new technologies to the mass production. This would require synchronisation activities between actors at different level of the value chain. For instance, addressing the needs of the automotive industry in WBG components would require the development of competitive and efficient components for the power conversion. The use of larger SiC wafer appears to be the key element in meeting the energy transition objectives of the Union. Furthermore, the coordination amongst actors at different levels of the value chain, from the material supplier to the end-users, will likely play an important role to mitigate the associated risks and foster, as a result, innovation. Given the lack of industrial-scale facilities, the related technologies are not currently available in the required wafer dimensions, and significant R&D&I and FID works are needed to reduce the associated technological risks.

(445) The development of advanced microelectronics and communication technologies furthermore faces financial and economic risks considering that the amounts involved in IPCEI ME/CT are significant. The financial risk is proportionate to the

high level of investment needed by the participating undertakings to advance their individual projects and relates also to the fact that IPCEI ME/CT establishes collaborations between actors of different size, structure and financial capacity. Mobilising State aid in a synchronised manner for all participating undertakings is expected to reduce the financial risk, either directly, thanks to the direct grants provided by the Member States, or indirectly, by easing the access to private co-financing.

(446) IPCEI ME/CT, moreover, entails economic risks stemming from the mismatch between the development of new technologies and the ability of industries to integrate them into the products and services that are currently available on the market. The Commission notes that the microelectronics market is generally uncertain and at the same time, capital and human resource intensive, with a high share of R&D&I activities. ([41]) This uncertainty may lead the participating undertakings limit the potential losses, as a consequence of those associated risks, by postponing their R&D&I and FID efforts, for instance. The development of smart SiC technology in WS-ACT to substitute very expansive SiC substrates, illustrates this situation: the development of this technology, which is highly beneficial to the deployment of WBG components for automotive applications, and generally to the green transition, requires an important effort in terms of R&D&I and investment in a market that is driven by competition. As a consequence, the associated applications would be exposed to an economic risk in case of delay in the R&D&I and FID phases.

(447) The participating undertakings furthermore will face strategic and organisational risks. The implementation period of IPCEI ME/CT and of the individual projects will be lengthy, and numerous changes of the projects' operating conditions are very likely to occur. The planned collaborations and synergies between multiple different stakeholders from various sectors, are expected to entail challenges and synchronisation of time schedules between all actors involved (i.e., participating undertakings, associated undertakings and indirect partners) is of paramount importance. For instance, deploying the WBG technology in the automotive sector, would require the prior consideration of constraints in the definition of substrates and components. In addition, the future deployment of 6G, would require the active and synchronised involvement of different actors of the microelectronics and communication technologies value chain, from the raw material suppliers (e.g., Si- or GaN-wafers and substrates) to the future 6G integrators (e.g., Nokia-DE, Nokia-FI, Ericsson etc.) through the semiconductor manufacturers (e.g., GF, IFX-AT, IFX-DE, NXP-AT, NXP-DE, STM-FR etc.) and ROs in the different WS.

(448) All of the above-mentioned risks that the participating undertaking are confronted with during the implementation of their individual projects, demonstrate the importance of IPCEI ME/CT as a whole. The Commission considers that the IPCEI ME/CT is designed in such a way to enable the participating undertakings to overcome or at least minimise those risks. For example, the sharing of best-practices, know-how and results through the multiple collaborations established within IPCEI

([41]) Commission Staff Working document, *A chips Act for Europe*, SWD(2022) 147, 11.5.2022; BCG x SIA, *Strengthening the global semiconductor supply chain in an uncertain era*, April 2021; and, *Business enterprise expenditure on R&D as a share of gross valued added, 2018 (or nearest year)*", in Health at a Glance 2021: OECD Indicators, OECD Publishing, Paris; and, *Measuring distortions in international markets: The semiconductor value chain*, 2019 OECD, Paris.

ME/CT, as well as with associated participants and indirect partners, aim to enable the participating undertakings overcome the technological risks involved, as well as find early adopters of innovative technologies with reduced level of risks, thereby accelerating the implementation of the individual projects and minimising the economic or financial risks that potential delays would have created. In addition, IPCEI ME/CT is expected to contribute to providing access to industrial capacities to innovative companies, especially SMEs, thereby contributing to alleviating the risk for these actors stemming from potential absence of collaborative interactions that would support and accelerate the development of their innovative projects.

3.3.2.4. Conclusion on the eligibility of IPCEI ME/CT

(449) In view of the above, the Commission concludes that IPCEI ME/CT meets the eligibility criteria of the IPCEI Communication.

*3.3.3. Compatibility criteria*

(450) When assessing the compatibility with the internal market of aid to promote the execution of an IPCEI on the basis of Article 107(3)(b) TFEU, point 27 of the IPCEI Communication requires the Commission to take into account a number of criteria, as elaborated below in the present section. Moreover, point 28 of the IPCEI Communication also requires the Commission to carry out a balancing test to assess whether the expected positive effects outweigh the possible negative effects.

(451) The Commission analysed the compatibility criteria at the level of aid beneficiaries and per individual project.

3.3.3.1. Necessity and proportionality of the aid

Necessity of the aid

(452) According to point 30 of the IPCEI Communication, the aid must not subsidise the costs of a project that an undertaking would anyhow incur and must not compensate for the normal business risk of an economic activity. Without the aid, the realisation of the project should be impossible, or it should be realised in a smaller size or scope or in a different manner that would significantly restrict its expected benefits. According to footnote 26 of the IPCEI Communication, the application for aid must precede the starts of the works. According to point 31 of the IPCEI Communication, the Member State must provide the Commission with adequate information concerning the aided project, as well as a comprehensive description of the counterfactual scenario, which corresponds to the situation where no aid is awarded by any Member State.

(453) The Commission has verified that all undertakings have submitted their applications for aid to the relevant Member States before the start of the works on their individual projects included in IPCEI ME/CT, therefore the formal incentive effect criterion, as required by the IPCEI Communication (footnote 26) has been met.

(454) The Member States have submitted information demonstrating that the aid has a substantive incentive effect for all aid beneficiaries, i.e., that the aid will induce the beneficiaries to change their behaviour by enabling them to engage in their individual projects in their full ambitious scope and in the time span as notified. This information is revealed in the counterfactual scenarios for each of the aid

beneficiaries and by the insufficient rates of return, indicated by the negative net present value ("NPV") of the aided projects, in line with point 32 of the IPCEI Communication. Furthermore, the Commission verified that the aid is kept to the minimum necessary to ensure the implementation of IPCEI ME/CT (see recitals (461) to (501)).

(455) The Member States confirm that, absent IPCEI ME/CT public financing, each of the aid beneficiaries has demonstrated that it either: (i) would not undertake their individual projects and, for example, would continue technologically less advanced activities, (ii) if the beneficiaries would develop alternative projects, they would not undertake them with sufficient speed, or they would carry out activities with a significantly lower level of ambition, for example from an innovative or environmental point of view, or (iii) would merely await and import new technologies once developed from third countries.

(456) The Member States have underlined that absent the aid, the development of a competitive, innovative and stronger European microelectronics and communications ecosystem would not take place. The innovations both in terms of increased performance and reduced environmental impacts, would not be made available to consumers, as each participating undertaking would have focussed on its own, less ambitious programme.

(457) In view of the above, the Commission notes that the information provided by the Member States (e.g., reports, board presentations or minutes illustrating the choices, which the company contemplated at the time of deciding on the IPCEI ME/CT project), shows that in the absence of aid, the participating undertakings would not undertake their individual projects. Indeed, on the basis of the information provided by the Member States, there is no evidence showing that the participating undertakings had considered such projects in their internal decision-making at the time of taking the decision to apply for the public support. Further, an analysis of the factual and counterfactual scenarios in the context of the funding gap (as discussed in recitals (484) to (495)), shows that undertakings would not have had a financial incentive to implement their projects in the absence of aid. Thus, the absence of aid would seriously jeopardise the materialisation of IPCEI ME/CT.

(458) The Member States submit (also where the aid would not cover the funding gap (see recital (328)) that the aid induces the change of the aid beneficiaries' behaviour, in that the aid beneficiaries either obtain sufficient State aid to implement their individual project or make it financially stable to attract additional funding. That additional funding may be public, although interest from private investors in supporting an individual project under IPCEI ME/CT would still be expected even in cases where the funding gap is not entirely covered by State aid. The reasons for such private interest could be for instance, the lower perceived investment risk once IPCEI ME/CT is approved, the possibility of private investors contributing to the funding of individual projects that would offer them a technological competitive edge, or the expected positive impact that such contribution would have on the private investors' reputation. Those factors meaningfully influence the choices of private investors, nevertheless they are intangible and therefore difficult to incorporate in the funding gap calculation. To this end, the Commission considers that even where a limited proportion of the notified funding gap of individual projects remains uncovered by State aid, the approved State aid will induce the

change of beneficiaries' behaviour and prompt the implementation of the individual projects, with additional funding, if necessary.

(459) In its assessment of the eligible costs, the Commission verified that the list of submitted costs would not include costs that an undertaking would have incurred in any event, such as costs linked to already existing laboratories in which research would have been conducted anyhow and the undertaking would have had to support those facility and personnel costs, even without IPCEI ME/CT. In view of the above, the Commission considers that the Member States have sufficiently demonstrated that the aid measures do not subsidise the costs of projects that the participating undertakings would have incurred in any event and do not compensate for their normal business risks.

(460) Considering the fact that the aid measures enable the participating undertakings to pursue ambitious projects, which would not have been pursued in the absence of IPCEI ME/CT, the Commission concludes therefore that the notified aid measures are necessary to induce a change in the aid beneficiaries' behaviour in light of the section 4.1 of the IPCEI Communication.

Proportionality of the aid

(461) According to point 32 of the IPCEI Communication, in the absence of an alternative project, the Commission will verify that the aid amount does not exceed the minimum necessary for the aided project to be sufficiently profitable, for example by making it possible to achieve an internal rate of return corresponding to the sector or firm specific benchmark or hurdle rate. According to point 33 of the IPCEI Communication, the maximum aid level is determined with regard to the identified funding gap and to the eligible costs. The aid could cover all of the eligible costs, provided that the aid amount does not exceed the funding gap.

(462) The Member States have submitted, for all participating undertakings, detailed calculations of the eligible costs for their individual projects as well as detailed funding gap calculations.

Assessment of eligible costs

(463) In its assessment of the eligibility of the costs, for all the individual projects, the Commission verified that the eligible costs comply with those that are set out in the Annex to the IPCEI Communication. To this end, the Commission has assessed the eligible costs and funding gap calculations for each individual project and established a maximum permitted aid level for each individual project. In case the notified nominal State aid amounts were higher than the permitted aid level, the Commission verified for each individual project (using the WACC of the individual project as the discount factor) that the discounted values of the nominal State aid amounts do not exceed the maximum permitted aid levels.

(464) The Commission consistently verified for all of the individual projects participating in IPCEI ME/CT that a high innovation level is to be reached, and that the activities are not limited to merely enabling an incremental evolution of existing technologies embedded in microelectronics and communication technologies already existing on the market (see recitals (422) to (439)). Moreover, the Member States have verified that the related R&D&I costs of each aid beneficiary comply with the Annex on eligible costs to the IPCEI Communication. The Commission confirms that these

costs fall within the categories listed in points (a) to (h) as set out in the Annex to the IPCEI Communication. In line with points (b) and (c), if instruments and equipment or buildings and land are not to be used during their full useful life for IPCEI ME/CT, the Commission has verified that only the depreciation costs corresponding to the R&D&I and FID phases are considered for the calculation of the eligible costs. The Commission has also required that the aid beneficiaries demonstrate that the depreciation periods used correspond to good accounting practice generally applied by the participating undertakings.

(465) For the individual FID projects, the Commission verified, in order to determine whether they qualify as FID under the IPCEI Communication, that the FID activities:

a. concern "the development of a new product or service with high research and innovation content and/or the deployment of a fundamentally innovative production process" ([42]);

b. do not relate to "regular upgrades without an innovative dimension of existing facilities and the development of newer versions of existing products" ([43]);

c. consist in "the upscaling of pilot facilities, or [to] the first-in-kind equipment and facilities which cover the steps subsequent to the pilot line including the testing phase and bring batch production to scale";

d. do not correspond to mass production nor to commercial activities" ([44]);

e. relate to the capital and operating expenditures ("CAPEX" and "OPEX") to the extent and for the period used for the project, as long as the industrial deployment follows on from an R&D&I activity and itself contains a very important R&D&I component, which constitutes an integral and necessary element for the successful implementation of the project ([45]).

(466) Having regard to the specificities of the microelectronics and communication technologies value chain concerned and the participating undertakings' individual FID projects contained in IPCEI ME/CT, the Commission has assessed the eligibility of FID costs for each aid beneficiary according to the above criteria, as follows.

(467) The Commission's assessment took into account, for each FID project specifically, the integration of the microelectronics and communication technologies in systems and processes, their compatibility with the end-use applications, the technological complexity and performance going substantially beyond the global state-of-the-art of microelectronics and communication technologies, the applications addressed and their specific constraints in particular in terms of safety and reliability. When assessing the setting up of processes (e.g., setting up innovative, first-in-kind pilot facilities to integrate novel materials and designs in essential microelectronic

([42]) Point 23 of the IPCEI Communication, first sentence.

([43]) Point 23 of the IPCEI Communication, second sentence.

([44]) Point 24 of the IPCEI Communication.

([45]) Point (g) in the Annex to the IPCEI Communication. The wording of the IPCEI Communication implies that the very important R&D&I component that needs to be embedded in the FID costs in order for these to be eligible constitutes a limit both in scope and time ("as long as") on the eligible FID costs.

components and systems and gradually while testing, scaling the new production methods up at the required level of quality, efficiency, and reliability, etc.), activities were only considered eligible where they relate to the introduction of processes that transfer the R&D&I performed before, into the FID phase, and are critical for the functionality of the resulting product. These activities were assessed against the most up-to-date publicly available information related to the different IPCEI ME/CT technologies and systems (including scientific and technical literature journals, corporate technical scientific publications, patents, etc.).

(468) The Commission finds for all aid beneficiaries, for each FID project, that it concerns either a new product with high R&D&I content or a fundamentally innovative production process or both (see recitals (422) to (439)).

(469) The Commission further finds for all aid beneficiaries engaging in FID projects that each of those projects concerns technologies with high R&D&I content or that are of a fundamentally innovative nature. These highly innovative technologies result from a preceding R&D&I activity, but they still require additional important R&D&I to be carried out, even after the R&D&I phase (e.g., to scale up and optimise the processes and first-in-kind equipment to make them meet the requirements for going into mass production, such as reliability and efficiency of the production process, achieve the required quality of output, test and adapt the performance of the product and the pilot line on the basis of the technological feedback obtained from downstream industries). As such, the FID of these specific technologies contains an additional important R&D&I component on its own (quantitatively or qualitatively), which is indispensable for the successful FID of the technologies.

(470) In relation to the very important R&D&I component, the Commission finds that all of the beneficiaries have provided an adequate demonstration of the very important (in quantitative and/or qualitative terms) R&D&I activities in their FID, which constitutes an integral and necessary element for the successful implementation of their individual projects. In particular, the Commission verified that each FID project demonstrated that the planned important R&D&I during the FID is necessary to solve outstanding technological roadblocks, among others in terms of microelectronic and communication technologies integration, design stability, cost-effective automatised processes, testing and validation, safety and reliability of materials and components, in the context of the complex technologies and large number of processes involved. In particular, the assessment of the very important R&D&I component in the FID of each aid beneficiary took into account the following elements.

(471) In its assessment, the Commission verified, on the basis of the parameters established in recitals (465) and (466), that the FID is not a mere regular upgrade, without an innovative dimension, of existing facilities, or a development of newer versions of existing products or technologies. Mere engineering work accompanying normal activities of FID does not constitute eligible costs for the required R&D&I in FID.

(472) In its assessment, the Commission further considered that where FID costs and the embedded R&D&I do not relate to the highly/fundamentally innovative technologies the beneficiary is developing, these are not eligible. Where the R&D&I in FID does not take place before the end of FID (end date in line with the IPCEI Communication), the FID costs are not eligible. The Commission has verified that

such R&D&I costs are excluded from the eligible costs represented in Tables 7 to 20, under recital (328).

(473) The Commission moreover verified that the FID as described by the Member States for the different aid beneficiaries does not cover mass production or commercial activities.

(474) In this context, the Commission first examined whether the different beneficiaries established KPIs (e.g., quality of product, durability, compatibility, energy consumption, safety, environmental impact, etc.) for identifying the moment in time when they reach a stabilised mass production. Any costs relating to the development occurring after the KPIs have been met cannot be included in eligible FID costs. The Commission verified that they were not included in the eligible costs represented in Tables 7 to 20, under recital (328).

(475) Furthermore, the Commission verified that the activities taking place during the FID phases notified by the Member States for the different participating undertakings correspond to FID activities and not mass production or commercial activities. Thus, in addition to verifying that the FID phases are accompanied by a significant R&D&I effort until the end of FID, the Commission also verified that the activities undertaken during these periods do not correspond to commercial activities both in quantitative and qualitative terms.

(476) In performing this verification, the Commission identified an FID phase as corresponding to a phase in which the undertaking starts to test the production of its new product or the new production method outside the lab and the pilot plant. Undertakings provide pre-commercial samples to selected potential customers to verify the quality of the sample and how it can be integrated in the potential customers' activities. Typically, at that moment, new issues will appear, and the sample-product might need to be changed or the production process might need to be modified or further developed. During the FID, numerous trial runs and a critical number of testing scenarios will be performed at different days and shifts to validate the production process with many idle moments in between. This validation process is particularly important and needed in the development of microelectronics and communication technologies, due to the close alignment between the microelectronics systems' design and architecture and its performance in the given application. Further, high demands on quality and reliability of the microelectronics components lead to a careful calibration of the production process. Therefore, the initial, limited sales during FID aim at obtaining a necessary feedback looped back into additional R&D&I efforts and the preparation of a subsequent stable process, with the proportion of faulty items reduced to minimum, before the production process can transition to mass production after the end of the FID phase (see (428)).

(477) In addition, as the activities supported under IPCEI ME/CT involve substantial innovations, the FID activities (including testing, sampling and upscaling) continue to involve an important R&D&I effort until the end of FID, which the Commission has verified, as indicated under recital (470)). During the ramp-up period, given that the production processes are put in place for the first time, complications are expected, and adjustments will in any event be needed to remedy the situation, potentially requiring that part of the production process to be redesigned.

(478) Even during the upscaling, potential customers expect the delivery of sample-products of a sufficiently high quality to be used for their own needs and requirements. In the FID phase, this cannot be achieved at arms' length. Customers will be particularly keen to require extensive liabilities from new entrants. Those quality assurances imply for the undertakings, additional quality control, screening and sorting processes, which are not needed once the production process has stabilised and would also not be sustainable under normal commercial conditions (because they are too costly). During the FID phase, customers reserve the right to reject or return shipments not only in the event of a quality issue but also in cases that customer applications show technical problems, or the market introduction is postponed, in particular from new entrants.

(479) The Commission verified that the planned FID activities included by Member States in the eligible costs calculations presented in Tables 7 to 20, under recital (328): a) correspond only to the testing, sampling and upscaling activities described in recitals (476) to (478), b) include only activities that still require significant R&D&I effort, c) correspond only to a limited output volume, and d) when a small volume of sales is planned, those sales occur under extended liability conditions. Conversely, the Commission verified that sales occurring after product qualification and years for which high volumes of sales were already planned were not included in the FID and excluded from the eligible cost calculations summarised in Tables 7 to 20, under recital (328), given that such sales would point to commercial activities. ([46])

(480) The Commission's assessment confirms that the notified FID phases of all aid beneficiaries comply with the requirement of the IPCEI Communication not to cover either mass production or commercial activities and that the costs summarised in Tables 7 to 20, under recital (328), for the FID phase of each beneficiary relate to FID within the meaning of the IPCEI Communication.

(481) With regard to the eligible FID costs, the Commission also verified that for cost items that are depreciated during several years, only depreciation costs until the end of the FID phase are included in the eligible costs. The Commission further required the aid beneficiaries to demonstrate that the depreciation periods used correspond to good accounting practice generally applied by the participating undertakings.

(482) With regard to the operating costs, which should be limited both in scope and in time to the R&D&I that the FID entails according to the Annex to the IPCEI Communication, the Commission examined thoroughly the costs information provided by the Member States and considers the requirement to have been fulfilled, because it has found that the operating costs constitute an integral and necessary part for the implementation of the R&D&I and FID activities of the individual projects.

(483) The Commission moreover generally reviewed the cost information provided by the Member States and summarised in Tables 7 to 20, under recital (328), and considers that they fulfil the conditions set out in the Annex to the IPCEI Communication. Based on the above, the Commission finds that the costs notified by the Member States in relation to all aid beneficiaries constitute eligible costs for IPCEI ME/CT and fulfil the requirements of the Annex to the IPCEI Communication.

([46]) According to footnote 24 of the IPCEI, "[l]imited sales, when necessary, in the specific sector, related to the testing phase, including sample or feedback or certification sales, are excluded from the notion of 'commercial activities'".

Assessment of funding gaps

(484) The Commission reviewed in detail the funding gap calculations provided by the Member States for each aid beneficiary and verified the main assumptions in those calculations, as explained below.

(485) In the absence of credible, sufficiently substantiated alternative project, the funding gap, as set out in point 33 of the IPCEI Communication, is equal to the difference between the positive and negative cash flows over the lifetime of the investment, discounted to their current value on the basis of an appropriate discount factor reflecting the rate of return necessary for the beneficiary to carry out the project. The reference to the lifetime of the project means that the funding gap includes also the financial streams related to the mass production following from IPCEI ME/CT. The cash flows are discounted at the WACC of the aid beneficiary.

(486) The Commission assessed the funding gap of each project at the level of each aid beneficiary. This assessment comprises:

- first, an analysis whether point 34 of the IPCEI Communication is applicable. More specifically, whether the beneficiary faced a clear choice between carrying out either an aided project or an alternative one without aid (counterfactual scenario), which would be sufficiently specific to justify including the information on the expected NPV of the counterfactual project into determination of the aid proportionality; and

- second, reviewing and verifying the funding gap assumptions.

(487) Regarding the analysis of the alternative scenario's existence, the Commission verified whether the information on the alternative project in the absence of aid each undertaking provided a credible, specific and substantiated counterfactual scenario. For the counterfactual scenario, the Commission observes that the participating undertakings have reported the following options, in the absence of IPCEI ME/CT:

- one third of the participants would undertake no alternative project at all and would continue business as usual, which for instance means offering their existing level of energy efficiency or performance; and

- two thirds of participants would undertake a project in a similar technological area, somewhat comparable to the project under IPCEI ME/CT, but with a different scope (e.g., delayed, smaller in size, lower level of technological ambition, for instance related to waiting for third parties to develop relevant technology and licencing it, when it proves sufficiently commercially attractive, etc.) or in a location outside of Europe.

(488) Where the counterfactual scenario consisted in no alternative project at all or the alternative course of action was not sufficiently precise (e.g., waiting for the market to develop, relying on third parties to develop relevant technologies and licence them) to be quantified, the Commission, following an assessment of all the relevant information and financial data provided by the Member States, did not find grounds for the application of point 34 of the IPCEI Communication.

(489) In few cases, where the undertakings claimed to face a clear choice between aided project and an alternative one, and further provided positive NPV calculations for the alternative project, the Commission first analysed whether the alternative project is sufficiently specific, credible and substantiated. Due to the lack of substantiation in form of relevant, contemporary internal company documents (e.g., reports, board presentations or minutes illustrating the choices, which the company contemplated at the time of deciding on the IPCEI ME/CT project), the Commission concluded that information provided on the financial aspects of the counterfactual scenarios was not specific and reliable enough to apply point 34 of the IPCEI Communication. As a result, it did not compare the expected NPV of the investment in the aided project and the counterfactual project for the purpose of determining the proportionality of aid.

(490) In the second step, the Commission reviewed and verified the funding gap assumptions for the factual scenarios. Particular scrutiny was applied to the revenues, terminal value and WACC assumptions.

(491) First, the Commission assessed and ensured that the projections of each individual project include all of the revenues expected to be generated from their respective investments. To this end, the Commission verified that the revenue streams:

- are comprehensive and thus in line with the technical characteristics of each of the individual projects;
- accrue over the entire lifetime of the investment and span over the expected life cycle of the respective project; and
- lead during the project's lifetime to a profit margin in line with the market.

(492) Second, the Commission verified and ensured that each individual project's projections include a terminal value that captures any remaining expected market value of the project after the end of the projections.

(493) Third, the Commission verified that each individual project's WACC:

- corresponds to each undertaking's internal WACC. Deviations from this rule were assessed on a case-by-case basis.
- is calculated by applying the formula below:

$$WACC = \frac{E}{D+E} * \left(r_f + \beta * ERP\right) + \frac{D}{D+E} * (r_f + DP) * (1 - T),$$

where: E = equity, D = debt, $r_f$ = risk-free rate, β = equity beta, ERP = equity risk premium, DP = debt premium and T = tax rate, and all of the parameters in the formula above, together with their sources and the methodology to determine them are provided.

- is in line with external benchmarks. To this aim, the Commission has identified benchmarks for the WACC's parameters based on publicly available data, with the aim of assessing the plausibility of the WACC. ([47])

(494) Having verified compliance with each of the above elements for each of the individual projects, the Commission concludes that all participating undertakings have calculated their funding gap in line with the IPCEI Communication and guidance provided.

(495) The Commission observes that both the eligible costs and the funding gaps have been calculated in line with the IPCEI Communication, and that the notified aid amounts do not exceed the minimum between the funding gap and the eligible costs (as reported in section 2.6.2).

Claw-back mechanism

(496) The Commission notes that the vast majority of individual projects will be subject, also in light of the very large aid amounts involved, to a claw-back mechanism, described in section 2.8 and in Annex I, which provides, in line with point 36 of the IPCEI Communication, an additional safeguard to ensure that the State aid remains proportionate and limited to the minimum necessary.

(497) In particular, by limiting to 60% the share of the extra profitability that can be clawed-back by the Member State (see Annex I), the claw-back mechanism notified by the Member States ensures, as provided for by point 36 of the IPCEI Communication, a balanced distribution of additional gains when the project is more profitable than forecasted and maintains strong incentives for beneficiaries to maximise their investment and project performance.

(498) Furthermore, the claw-back mechanism notified by the Member States will apply only to those investments which reach, based on the *ex post* cash flow results and of State aid disbursements, a rate of return exceeding the beneficiaries' cost of capital (specifically the beneficiaries' WACC, see Annex I).

(499) The Commission further notes that the IPCEI Communication recognises that it may be appropriate to take steps to ensure that the claw-back mechanism does not result in disproportionate burdens. In this respect, footnote 30 of the IPCEI Communication, states that "[f]or projects by SMEs, no claw-back mechanism needs to be implemented unless in exceptional circumstances, in particular in consideration to the amounts of aid notified for such projects". In IPCEI ME/CT, notwithstanding their size, some SMEs will be granted very large amounts of aid, in excess of EUR 50 million, which exceeds their turnover. This amount can be deemed an exceptional circumstance considering that, in order to qualify as an SME under the relevant Union definition ([48]), the enterprise's annual turnover must not exceed EUR 50 million. In this light, the Commission considers that, in the present circumstances, a claw-back mechanism which is limited by reference to the amount of the notified aid,

([47]) The benchmarks identified by the Commission reflect the country and industry risks of the individual projects.

([48]) See Annex I of Commission Regulation (EU) No 651/2014 of 17 June 2014, declaring certain categories of aid compatible with the internal market in application of Article 107 and 108 of the Treaty, OJ L 187/1, 26.6.2014.

per participating undertaking per Member State , is more appropriate to avoid disproportionate administrative burdens than a mechanism based on the size of the relevant participating undertaking. Consequently, the Commission considers it appropriate for the claw-back mechanism to apply also for individual projects by SMEs, where the notified aid amount is higher than EUR 50 million.

(500) In addition, where the notified aid may be cumulated with aid under other measures, Member States have put in place mechanisms to make sure that irrespective of the source of the funding (local, regional, national or Union funding), the total public support will not exceed the notified and approved aid amount under this decision.

(501) Therefore, the Commission considers that the aid to be granted by the notifying Member States is proportionate.

3.3.3.2. Prevention of undue distortions of competition and balancing test

Appropriateness

(502) According to point 42 of the IPCEI Communication, the Member State must provide evidence that the proposed aid measure constitutes the appropriate policy instrument to address the objective of the project.

(503) The Member States submit that State aid is the appropriate policy instrument to support IPCEI ME/CT. In their view, due to the exceptional size of IPCEI ME/CT and the synergies it requires from the various partners, it could not be achieved without the support of the Member States involved in the financing of IPCEI ME/CT. Alternatively, the participating undertakings would not deliver breakthrough innovations whose spillover effects largely benefit the Union ecosystem.

(504) The Member States further argue that the payment of direct grants constitutes the appropriate instrument in view of the high risk of IPCEI ME/CT in financial and technological terms and the low expected profitability induced by the relevant spillovers. Furthermore, Member States submit that direct grants address the coordination problems and encourage the participating undertakings to commit to their projects for the achievement of common objectives.

(505) The Commission shares the views of the Member States that given the level of risks and the ambitions pursued by IPCEI ME/CT, its size and numerous collaborative interactions that it will induce, the public support through the notified State aid measures constitutes the appropriate policy instrument to address the objectives of IPCEI ME/CT. In the view of the Commission, the use of repayable advance does not constitute an appropriate aid instrument in cases such as the one at hand, whereby the microelectronics and communication technologies industry is cyclical and experiences short-term downturns, ([49]) while the success of individual projects depends to a large extent on the implementation of coordinated actions of all of the participating undertakings.,. Considering the market failures identified, in particular the need to address the coordination problems and asymmetric information involved (see recitals (376) to (380)), and taking into account the level of risk and uncertainty

([49]) Despite Short-Term Cyclical Downturn, Global Semiconductor Market's Long-Term Outlook is Strong - Semiconductor Industry Association (www. semiconductors.org).

(see recitals (442) to (448)), the Commission considers the use of direct grants to be appropriate, pursuant to point 40 of the IPCEI Communication.

Identification of the potential risks of distortions of competition

(506) According to point 43 of the IPCEI Communication, aid can be declared compatible if the negative effects of the aid in terms of distortions of competition and impact on trade between Member States are limited and outweighed by the positive effects in terms of contribution to the objective of common European interest. The assessment of the potential negative effects of the aid under the IPCEI Communication needs to consider, in particular, the effects on competition between undertakings in the markets concerned, including up- or downstream markets, the risk of overcapacity, as well as risks of market foreclosure and dominance (points 44 and 45 of the IPCEI Communication).

(507) The Member States provided detailed information and reasoning on the absence of undue distortions to competition in relation to each individual project under the IPCEI ME/CT. In particular, the Member States argue that the broad semiconductor market is expected to steadily increase in the coming years, as illustrated in Figure 4:

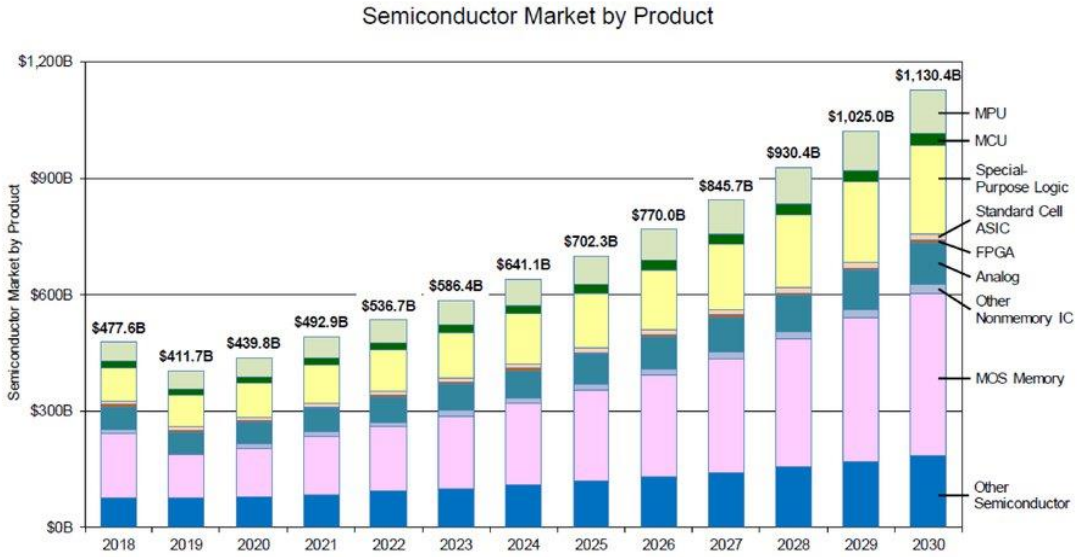


***Figure 4: Semiconductor market by product from 2018 to 2030(source IBS 2022)***

(508) In addition, according to the Member States, Europe has a limited presence in the semiconductor chips market with around 10% of global revenues, compared to the 20% of the 1990s. The Member States submit that the markets or sectors, where a stronger market position of few participating undertakings were identified are as follows:

| WS | Markets with strong EU presence |
|---|---|
| SENSE | MEMS, photodiodes, image sensors, LiDAR, industrial sensors, ADAS |
| THINK | MCU, processors for automotive, ASIC |
| ACT | Power components, power modules |
| COMMUNICATE | RF components, RF modules, Radio telecommunication equipment, optical communication equipment, broadband digitisers (data converters) |

***Table 28: Markets for assessment in terms of foreclosure and dominance***

(509) In the few cases of participating undertakings already active in the markets illustrated in Table 28, the Member States argue that there should be no concerns of undue distortions of competition, given that the current and expected market shares of the participating undertakings already active in these markets are not material and State aid will not strengthen their market position any further. The Member States furthermore indicate that there will be no risk of foreclosure and overcapacity as a consequence of IPCEI ME/CT, given that the demand for microelectronics systems and devices is expected to grow strongly by 2030 (see Figure 4).

(510) The Commission's analysis of undue distortions to competition is specific to the particular case at hand. The assessment of potential distortions to competition was carried out taking into account the particularities of the WS concerned and the participating undertakings involved. The assessment of the potential negative effects of the aid under the IPCEI Communication needs to consider, in particular, the effects on competition between undertakings in the concerned product markets, as well as risks of market foreclosure and dominance.

(511) The assessment of distortions to competition has followed a consistent approach across all individual projects, while each project was in addition assessed individually in detail by the Commission. IPCEI ME/CT involves a large number of participating undertakings, each with a current or future presence across the whole microelectronics and communication technologies value chain. For this reason, as it has been the practice in similar cases, ([50]) in this particular case, the Commission adopted a two-step approach, as described below, in order to identify potential significant competition distortions that might result from the aid measures.

(512) In the first step, the Commission screened the individual projects based on indicators for assessing the potential distortive effects of State aid granted to the participating undertakings under IPCEI ME/CT, including the assessment of the position of these undertakings in the markets affected by IPCEI ME/CT and the amount of State aid granted to the respective undertakings, both in absolute and in relative terms.

([50]) SA.46578 (2018/N) and others - Important Project of Common European Interest (IPCEI) – Microelectronics, OJ C 7, 10.1.2020, p. 1; and, SA.56606 (2020/N) Austria joining the IPCEI Microelectronics 2018 (not yet published).

(513) In particular, the Commission screened participating undertakings' position based on a uniformly available metric on European production (the "PRODCOM" statistics on the production of manufactured goods collected by the Member States) ([51]). The Commission requested and received data on the aid beneficiaries' past production values by 8-digit PRODCOM classification for the product categories related to the aided projects in IPCEI ME/CT. Based on this information, the Commission assessed the share in the total EEA production of the respective undertakings involved in the project in the sectors as defined by the PRODCOM classification.

(514) This assessment was further developed by adapting it to the particularities of the sectors concerned and the participating undertakings involved. In particular, the assessment considered the segments affected by IPCEI ME/CT, specific for each WS, as illustrated in Figure 4 and Table 28. This allowed the assessment to be tailored to the markets affected by each aid measure concerned. In particular, the Commission requested and received data on the past turnover of both aid beneficiaries' and the overall segment for all segments of activity specific to each WS and related to the projects in IPCEI ME/CT, both at EEA and worldwide levels. In addition, for each segment and geographic level, the Commission requested and received data on aid beneficiaries' five main competitors. Based on this information, the Commission assessed whether undertakings are currently active in the segments in which they intend to develop the technologies for their eventual products, as a result of the aid measures at hand, and, if so, the share of the respective undertakings involved in the overall EEA and worldwide turnover in the respective segments.

(515) Consequently, the Commission followed a conservative approach in assessing segment shares of undertakings, as it has undertaken its assessment both at broader (segments of works-streams) and finer (PRODCOM) industry classifications.

(516) In addition, the Commission assessed the amount of State aid granted to the respective undertakings, considering both the absolute amount, as well as the relative amount as compared to the undertakings' and total turnover generated in the segments in which they intend to develop the technologies for their eventual products.

(517) This first step of the assessment allowed identifying individual projects where there might be risks of dominance and foreclosure by the strengthening or the maintaining of substantial market power by the aid beneficiaries. To this end, the Commission notes, as verified in its assessment of eligible costs (see recitals (458) to (490)), that IPCEI ME/CT does not cover funding for commercial activities and mass production, thereby mitigating the risk of dominance and foreclosure. Moreover, there are only limited sectors, where European undertaking have important market shares, although all of sectors are dominated by undertakings from USA, Taiwan, China and Korea. ([52])

([51]) Please note that the PRODCOM classification provides statistics on the production of manufactured goods by enterprises in Union countries, covering the economic activities of mining and quarrying, manufacturing, and materials recovery. As such, it does not cover economic activities in communications, which are the focus of a number of IPCEI ME/CT projects. In addition, it does not provide production values of manufactured goods outside of the Union, thereby not allowing to assess segment shares of undertakings in IPCEI ME/CT at the worldwide level.

([52]) IC Insights Q2-2022.

(518) In the second step, the Commission carried out an overall assessment of competition distortions based on the information provided for each participating undertaking by the relevant Member State. For those participating undertakings and projects raising potential concerns based on their position in the markets affected by State aid to IPCEI ME/CT, the Commission further assessed, based on the information provided in the notified project portfolios, whether other competitors active in the EEA markets, which may or may not have benefitted from public support, could be in any way foreclosed by the participating undertakings. Following that detailed analysis, the Commission observes that all concerned participating undertakings will receive the aid, which represents a limited proportion of their turnover in the respective segments affected by their individual projects (with the exception of one participating undertaking , for which the proportion of aid to the turnover in the Union amounts to 17%, The Commission furthermore observes that the proportion for all other cases does not exceed 10% and for majority of cases falls in the range 0,5% to 5,5% compared to the turnover in the EU and the range of 0% to 3% compared to the global turnover). Therefore, the potential to unduly strengthen their market position is rather limited. Moreover, the Commission considers that the risk of foreclosure is sufficiently addressed by the commitments to licence the IP resulting from their individual projects at FRAND terms and to grant access to the FID results by MPWs, access to facilities, workshops and test kits.

(519) The Commission furthermore assessed the potential risk of overcapacity and considers that the aid granted under IPCEI ME/CT will not support a declining market, based on the information provided by the Member States, and the fact that the individual projects address directly the challenges posed by the green and digital transitions and the ambition of the Union Green Deal for climate neutrality by 2050.

(520) The Commission also assessed the risk of a subsidy race between Member States, which may arise in particular with respect to the choice of location pursuant to point 46 of the IPCEI Communication. It must be noted in this regard that the national calls launched for preselecting potential projects (see recital (2)), as well as the demonstration of an open procedure for Member States to participate in IPCEI ME/CT (see recital (390)), have mitigated any such risk.

(521) Finally, the Commission notes that the Member States confirmed in their notifications that their respective aid measures are not conditional on the relocation of a production activity or any other activity of the beneficiary from another Contracting Party to the EEA Agreement to the territory of the Member State granting the aid, pursuant to point 47 of the IPCEI Communication.

(522) Following the assessment described above, the Commission has undertaken a balancing test to assess whether the expected positive effects of the aid outweigh its possible negative effects. The positive effects of the aid considered in the balancing test included concrete contributions of the individual projects under IPCEI ME/CT to addressing well-defined market failures (see recitals (372) to (387)), as well as the objectives of the common European interest (see recitals (362) to (371)).

(523) Furthermore, as far as the potential negative effects in terms of market dominance and foreclosure are concerned, the Commission shares the Member States' view that the market position of the participating undertakings will not be strengthened because of State aid, especially given the limited amount of such aid compared to their revenues. The Commission considers in this regard that, involving the

participating undertakings, particularly the larger ones, in IPCEI ME/CT, will enable them to establish important collaborative interactions among themselves and jointly contribute to the development of advanced products and processes for multiple downstream applications (see recitals (417) to (418)), thereby mitigating any risk of creating or strengthening existing market power. In addition, the Commission notes that any potential risk of dominance is mitigated by the participating undertakings' commitments to disseminate R&D&I and FID results (see recitals (394), (395) and (398)) and to unconditionally license IP-protected results of the funded projects based on FRAND conditions (see recitals (396) to (397)). Moreover, in view of the fact that the microelectronics market is expected to expand significantly, as illustrated by Figure 4 provided by the Member States, the Commission considers that the risks of IPCEI ME/CT giving rise to concerns based on overcapacity are limited. Lastly, the Commission stresses that the open and non-discriminatory procedure designed by the notifying Member States for the preselection and final selection of the participating undertakings in IPCEI ME/CT enabled all interested undertakings active in the relevant markets and segments thereof, to join IPCEI ME/CT, thereby minimising any potential risk of competition distortions. Equally, the fact that the aid measures are not conditional on the relocation of any activities ensures that no harm to the internal market occurs in this regard.

(524) The analysis of the detailed information available to the Commission, therefore, leads to the conclusion that the risks of foreclosure, dominance and overcapacity are likely to be outweighed by the positive effects of IPCEI ME/CT (see recital (441)).

3.3.3.3. No breach of any relevant provision of Union law

(525) State aid cannot be declared compatible with the internal market, if the supported activity, the aid measure, or the conditions attached to it entail a violation of relevant Union law ([53]) (see recital (334)).

(526) Based on the information submitted by the Member States, the Commission has no reason to consider that IPCEI ME/CT would involve any breach of Union law.

(527) In light of the above, the Commission considers that IPCEI ME/CT does not infringe relevant Union law, and that the condition of point 10 (c) of the IPCEI Communication is fulfilled.

3.3.3.4. Transparency

(528) The transparency requirements, specified in section 4.3 of the IPCEI Communication, are fulfilled (see recital (340)).

*3.3.4. Conclusion on compatibility*

(529) Based on the assessment under the IPCEI Communication, the Commission concludes that the notified aid measures are compatible with the internal market pursuant to Article 107(3)(b) TFEU.

([53]) Judgement of 31 January 2023, *European Commission v Anthony Braesch and Others*, C-284/21 P, EU:C:2023:58, paragraph 96.

### *3.3.5. Reporting obligation*

(530) According to point 52 of the IPCEI Communication the execution of the project must be subject to regular reporting.

(531) As notified by the Member States, the execution of IPCEI ME/CT will be subject to annual reporting by the participating undertakings and the Member States. This reporting is three-fold:

- first, the participating undertakings will report annually the execution of their activities, as regards the advancements of their individual projects, the individually committed spillovers and the compliance with the principle of 'do no significant harm' to the national funding authorities and any other complementary activities with other EU initiatives, for example, or the Key Digital Technologies Joint Undertaking or the Horizon Europe programme. The reporting period will ideally reflect the Member States' annual reporting obligation towards the Commission;
- second, the Member States will provide annually a summary report (of the undertakings' execution of their activities) to the Commission. In accordance with the Member States' notifications, a template will be created by the PAB during its first meeting and evaluated by the Commission. The reporting will be scheduled based on the annual FG meetings. A detailed description on the reporting mechanisms will be defined after the initial FG meeting, as well as the respective reporting period; and
- third, the SB, which has the role of supervising the monitoring and implementation of IPCEI ME/CT as a whole (see recital (51)), will report annually to the Commission on the progress of IPCEI ME/CT (including through KPIs). The reporting period should ideally follow the reporting of the Member States to the Commission.

(532) Further, the concerned Member States have agreed to report to the Commission on the application of the claw-back mechanism (see Annex I).

(533) The Commission therefore considers that the reporting obligation on the execution of IPCEI ME/CT is fulfilled.

## 4. CONCLUSION

(534) In view of the above and in light of the notifications of the Member States, the Commission has decided:

- not to raise objections to the aid on the grounds that it is compatible with the internal market pursuant to Article 107(3)(b) TFEU.

If this letter contains confidential information which should not be disclosed to third parties, please inform the Commission within fifteen working days of the date of receipt. If the Commission does not receive a reasoned request by that deadline, you will be deemed to agree to the disclosure to third parties and to the publication of the full text of the letter in the authentic language on the Internet site: http://ec.europa.eu/competition/elojade/isef/index.cfm.

Your request should be sent electronically to the following address:
European Commission,
Directorate-General Competition
State Aid Greffe
B-1049 Brussels
Stateaidgreffe@ec.europa.eu

Yours faithfully,

For the Commission

Margrethe VESTAGER
Executive Vice-President

CERTIFIED COPY
For the Secretary-General

Martine DEPREZ
Director
Decision-making & Collegiality
EUROPEAN COMMISSION

## ANNEX I

### CLAW-BACK MECHANISM

The aid is capped in nominal terms by the notified and actual eligible costs. Member States will also ensure that the discounted value in 2023 terms of the aid (using the notified WACC as a discount factor) will not exceed the notified funding gap.

The claw-back mechanism will apply to those aid beneficiaries for which the notified aid amount, per Member State, is above EUR 50 million. ([54]) ([55])

The basis for the claw-back mechanism will be *ex post* figures, which have been subject to annual approval by an independent auditor. For this purpose, separate analytical accounting will be required from the aid beneficiaries in the relevant Member State for their individual project or projects.

*Letter of credit*

Starting from the second year following the completion of the eligible R&D&I/FID-phases for such individual projects and thereafter, at least every two years for individual projects with a projected mass production phase exceeding four years and, every year for individual projects with projected mass production phase of four years or less, until an "End date" ([56]), a test will be run ("test-run") ([57]). In each test run, a $Surplus_i$ for year "i" will be computed as the sum (positive or negative) of:

a) the net present value, interest-adjusted to year "i" (using the notified WACC as the interest-adjustment rate ([58])), of the actual audited post-tax cash flows (including Capex and additional benefits ([59]); and excluding financing cash flows) from start of works to year "i" ([60]); and

([54]) The threshold of EUR 50 million of aid amount is to be understood in nominal terms. If the aid eventually disbursed to the aid beneficiary per Member State is lower than EUR 50 million, also in nominal terms, the aid beneficiary will be relieved from the claw-back mechanism. In such case, the Member State disbursing the aid commits to inform the Commission of the occurrence of a lower than the notified aid amount and of the inapplicability of the claw-back mechanism within 2 months after final disbursement of the aid.

([55]) Notified individual project(s), which subsequently are clearly determined as unsuccessful by both the aid beneficiary and the Member State – in particular, with regard to entrepreneurial decisions (e.g., the notified technology will not be pursued further) or due to financial reasons (e.g., the aid beneficiary cannot raise his own share) and are thus terminated before the end of R&D&I/FID phase, will not be subject to the claw-back mechanism. In such a case, the Commission would be informed by the Member State concerned within two months following the decision to terminate the notified individual project/projects.

([56]) The End date for the purposes of the claw-back mechanism is in principle set at the year corresponding to the last year that has been considered in the notified funding gap analysis for the relevant individual project. For individual projects with projected mass production phase exceeding ten years, the End date is set at the end of the tenth year. In the event of delays in the implementation of the individual projects compared to the notified schedule, the "End date" will be extended accordingly.

([57]) Each test-run must be completed no later than six months following the end of the respective testing period. This means that, for instance, if the testing period runs from 2026 to 2032 (i.e., two years following the completion of the eligible R&D&I/FID phases), the test-run must be completed by 30 June 2033.

([58]) This means that, for instance, for a test-run in 2028, a cash flow in 2023 will be multiplied by (1+WACC)^(5).

([59]) For the purpose of the claw-back mechanism, "additional benefits" mean additional public financial contributions – including any other State aid or public funding received – in relation to the same eligible

b) the net present value interest-adjusted to year "i" (using the notified WACC as the interest-adjustment rate) of the actual State aid disbursements from start of works to year "i"[60].

$Surplus_i$, if it is positive, will be multiplied by an allocation ratio $ShareState_i$ defined as the lesser between 60% or the net disbursed State aid from start of works to year "i" divided by the verified eligible costs from start of works to year "i" (both expressed in nominal terms).

The claw-back mechanism only applies in case of positive net present values of cash flows after taking into account the actual State aid disbursements.

A letter of credit (by a reputable financial institution having investment grade rating from a first-rank rating agency) should cover the repayment obligation at the End date by the aid beneficiary, from the first test-run.

The secured amount guaranteed by the above-mentioned letter of credit should be at least equal to an amount ensuring that the two following principles are fulfilled:

1) The secured amount must never be negative (initial balance equal to zero);

2) The secured amount must, after each test-run, correspond to the lower of the following, if positive:

- the $Surplus_i$ multiplied by $ShareState_i$ (computed at that test-run)

- The sum of the actual State aid disbursements between 2023 and that test-run expressed in terms of the year "i" of the test-period. For all the disbursements before that test-run, the discount factor will be the Union reference rate applicable to the Member State concerned according to the Commission's communication on setting the reference and discount rates ([61]) applicable at year "i", increased by 100 basis points, between the corresponding disbursement and year "i".

An amount equal to the final secured amount, after the last application at the End date, will be transferred to the Member State.

The application of the claw-back mechanism will be reported by the relevant Member State to the Commission within two months following completion of each test-run and after the End date.

*Account with annual transfers*

Alternatively, the Member State, instead of the letter of credit system described above, may opt for an account-based system. This system will apply exclusively if the two following conditions are both met: a) the account to be used for the purpose of applying the claw-back mechanism is not under the control of the aid beneficiary; and b) computations and transfers to/from the account by the aid beneficiary must take place at least every two years for

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costs of the notified individual project/projects for each aid beneficiary that were not part of the State aid notification.

(60) In cases where inputs and outputs are based on a transfer pricing methodology for intra- group transactions, the methodology included in the State aid notification of the individual projects continues to apply.

(61) OJ C 14, 19.1.2008, p. 6.

individual projects with projected mass production phase exceeding four years and, every year for individual projects with projected mass production phase of four years or less, until the End date. ([62])

The balance of that account should never be negative and no transfer by the Member State to the account shall take place at any time.

This account-based system must not be more favourable from the aid beneficiary perspective than the letter of credit system ([63]) and should ensure comparable results.

The annual application of the claw-back mechanism will be reported by the relevant Member State to the Commission within two months following completion of each test-run.

[62] The transfers to/from the account must take place not later than within the two months following the test run.

[63] Excluding the specific administrative costs of a letter of credit, as well as fees and deposit interests related to an account.

## ANNEX II

### TABLE OF ASSOCIATED PARTICIPANTS

| Country | Name of Associated Participant | Type |
|---|---|---|
| Austria | Silicon Austria Labs | RO |
| Belgium | BelGan | Large undertaking |
| Belgium | Soitec Belgium N.V. | Large undertaking |
| Czechia | NXP Semiconductors Czech Republic s.r.o | Large undertaking |
| Czechia | UJP Praha a.s. | SME |
| France | CEA | RO |
| France | Murata | Large undertaking |
| Germany | Applied Materials GmbH | Large undertaking |
| Germany | Swissbit Germany AG | Large undertaking |
| Greece | AKRONIC P.C. | SME |
| Greece | Ansys Hellas | Large undertaking |
| Greece | Applied Materials – Think Silicon | Large undertaking |
| Greece | Nanometrisis | SME |
| Hungary | Tungsram | Large undertaking |
| Italy | CNR Department of Physical Sciences and Technologies of Matter | RO |
| Italy | Fondazione Bruno Kessler | RO |
| Italy | OPTOI s.r.l. | SME |
| Norway | Nordic Semiconductor | Large undertaking |
| Norway | SINTEF | RO |
| Latvia | Latvijas Mobilais Telefons | Large undertaking |
| Portugal | ATEP-AMKOR | Large undertaking |
| Portugal | PIC advanced | SME |
| Romania | Analog Devices Romania | Large undertaking |
| Romania | IMT Bucharest | RO |
| Slovenia | Beyond Semiconductor d.o.o. | SME |
| Slovenia | Elaphe Propulsion Technologies Ltd. | SME |
| Spain | DAS Photonics | SME |
| Spain | Derivados del Flúor, S.A.U. | Large undertaking |
| Spain | IPronics | SME |
| Spain | VLC-Photonics | Large undertaking |
| Spain | Vodafone | Large undertaking |
| Spain | Wooptix | SME |

# ANNEX III

## TABLE OF TECHNICAL ABBREVIATIONS

| Abbreviation | Meaning |
|---|---|
| µC | Microcoulomb |
| 2D | Two dimensional |
| 3D | Three dimensional |
| 3DFD | 3D Full Die |
| 5G | 5th Generation |
| 6G | 6th Generation |
| AAS | Advanced Antenna Systems |
| AC | Analog Converter |
| AD | Automated Driving |
| ADAS | Advanced Driver Assistance Systems |
| ADC | Analog to Digital Conversion |
| AFE | Analog Front-End |
| AFM | Analog Front-end Modules |
| AFM | Atomic Force Microscopy |
| AI | Artificial Intelligence |
| AIGaN | Aluminium Gallium Nitride |
| AP | Advanced Packaging |
| AR | Augmented Reality |
| ASIC | Application-Specific Integrated Circuit |
| ASPIC | Application Specific Photonic Integration Circuit |
| BCD | Bipolar-CMOS-DMOS |
| BiCMOS | Bipolar CMOS |
| BLDC | Brush-Less Direct Current |
| BMS | Battery Management System |
| BTS | Base station Transceiver System |
| CCAM | Cooperative Connected and Automated Mobility |
| CiM | Computing-in-Memory |
| CMOS | Complementary Metal Oxide Semiconductor |
| CPU | Central Processing Unit |
| DAC | Digital to Analog Conversion |
| DC-DC | Direct Current Converter |
| DCU | Digital Control Unit |
| DL | Deep Learning |
| DR | Direct reduction |
| DSP | Digital Signal Processor |
| DUV | Deep Ultraviolet |
| E/E | Electrical/Electronic |
| ECU | Electronic Control Unit |

| | |
|---|---|
| EDA | Electronic Design Automation |
| Edge-AI | Edge Artificial Intelligence |
| Edge-HPC | Edge High-Performance Computing |
| Edge-IoT | Edge Internet of Things |
| eMCP | Embedded Multi Chip Packages |
| ESD | Electro-Static-Discharge |
| EUV | Extreme Ultraviolet |
| EV | Electric Vehicle |
| FD-SOI | Fully Depleted Silicon on Insulator |
| FPGA | Field Programmable Gate Array |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| GEN | Generation |
| GHz | Gigahertz |
| GPU | Graphic Processing Unit |
| HAD | Highly Automated Driving |
| high-NA EUV | High-Numerical Aperture Extreme Ultraviolet High |
| HPC | High-Performance Computing |
| HV-Box | High Voltage Box |
| HW | Hardware |
| IC | Integrated Circuit |
| IGBT | Insulated-Gate Bipolar Transistors |
| IMC | In Memory Computing |
| Industry 4.0 | 4th industrial revolution |
| InGaAs | Indium Gallium Arsenide |
| InP | Indium phosphide |
| IoT | Internet of Things |
| IR | Infrared |
| IR MEMS | Infrared Micro-Electro-Mechanical Systems |
| ISA | Industrial Set Architecture |
| ISP | Image Signal Processing |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diodes |
| LiDAR | Light Detection and Ranging |
| LNO | Lithium Niobate |
| LNOI | Lithium Niobate on Insulator |
| LTO | Lithium Tantalate |
| MCM | Multi Chip Module |
| MCU | Micro-controller Unit |
| MEMS | Micro-Electro-Mechanical Systems |
| microLED | Micro Light Emitting Diode |
| MIMO | Multi-input Multi-output |

| | |
|---|---|
| ML | Machine Learning |
| mm | Millimetre |
| MMIC | Monolithic Microwave Integrated Circuit |
| mmW | Maximising Millimetre Wave |
| MOCVD | Metal Organic Chemical Vapor Deposition |
| MOEMS | Micro-Opto-Electro-Mechanical Systems |
| MOSFET | Metal–Oxide–Semiconductor Field-Effect Transistor |
| MPW | Multi-Project Wafer |
| MTP | Micro-Transfer-Printing |
| NA | Numeric Aperature |
| NETD | Noise Equivalent Temperature Difference |
| NIR | Near-infrared |
| nm | Nanometre |
| NTN | Non Terrestrial Networking |
| NVM | Non-Volatile Memory |
| OEM | Original Equipment Manufacturers |
| O-RAN | Open Radio Access Network |
| O-RU | Open Radio Unit |
| OSAT | Outsourced Semiconductor Assembly and Test |
| OSNR | Optical Signal to Noise Ratio |
| OTA | Over The Air |
| PCB | Printed Circuits Board |
| PCIe | Peripheral Component Interconnect Express |
| PCM | Phase-Change Materials |
| PDK | Process Design Kit |
| PIC | Photonic IC |
| PLP | Panel Level Packaging |
| pMUTs | Ultrasonic Piezo Devices |
| POI | Piezoelectric-on-Insulator |
| PVT | Pressure, Volume and Temperature |
| RAN | Radio Access Network |
| RISC-V | Reduced Instruction Set Computer V |
| SAW | Surface Acoustic Wave |
| Si | Silicon |
| SiC | Silicon Carbide |
| SIM | Subscriber Identification Module |
| SiN | Silicon Nitride |
| SiP | System-in-Package |
| SoC | System-on-a-Chip |
| SOI | Silicon-in-Insulator |
| subThz | Sub-Terahertz |
| SW | Software |

| | |
|---|---|
| TaC | Tantalum Carbide |
| TEM | Transmission Electron Microscopy |
| TFT | Thin Film Transitor |
| TPU | Tensor Processor Unit |
| TRL | Technology readiness level |
| TSV | Through-Silicon-Via |
| UAV | Unmanned Aerial Vehicle |
| UWB | Ultra Wide-Band |
| VCSEL | Vertical-Cavity Surface-Emitting Laser |
| VIPower | Vertical Intelligent Power |
| vORAN | Virtualized O-RAN |
| VR | Virtual Reality |
| WBG | Wide-BangGap |
| ZCU | Zonal Control Unit |