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In the published version of this decision, some information has been omitted, pursuant to articles 30 and 31 of Council Regulation (EU) 2015/1589 of 13 July 2015 laying down detailed rules for the application of Article 108 of the Treaty on the Functioning of the European Union, concerning non-disclosure of information covered by professional secrecy. The omissions are shown thus […]		PUBLIC VERSION This document is made available for information purposes only.

Subject: State Aid SA.46578 (2018/N) – Germany
State Aid SA.46705 (2018/N) – France
State Aid SA.46595 (2018/N) – Italy
State Aid SA.46590 (2018/N) - United Kingdom

Important Project of Common European Interest (IPCEI) Microelectronics

Sirs,

1. PROCEDURE

(1) On 10 October 2016, Germany and the United Kingdom ("UK"), followed by Italy on 11 October 2016 and by France on 12 October 2016, pre-notified the above mentioned measures concerning an important project of common

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European interest ("IPCEI") in the fields of microelectronics[1] on the basis of a common draft overall descriptive text (so-called "Chapeau" document), to be thereafter complemented with the detailed information on the project and its components as and when progress would be made in the discussions between Member States and companies on the set up of the project.

(2) The Commission requested complementary information by letters dated 18 November 2016 and 22 March 2017, to which the Member States replied by letters dated 13 January and 19 May 2017. Further information was requested on 12 July 2017. Meetings were held between the Commission services and the pre-notifying Member States on 12 October 2016 and 16 February 2017.

(3) On 4 January 2017, the German authorities informed the Commission of their intention to allow enterprises to start their works on the project after having submitted a complete aid application. No public funding was granted yet as it is subject to a formal approval by the Commission

(4) On 8 September 2017, the German authorities submitted a brief overview of the German companies intended to participate in the IPCEI Microelectronics project and an intended State aid amount. In November 2017, discussions started on the template documents to be submitted for each company participating to the IPCEI Microelectronics and on the documents describing the underlying projects.

(5) On 20 December 2017, the German authorities committed to the German aid beneficiaries[2] to award aid under the condition of approval of the aid by the Commission.

(6) In December 2017, the Commission services took the initiative to organise high level meetings and working group meetings at technical level in order to enhance coordination between Member States and ensure progress in the delivery of information on the underlying projects in the prenotification stage.

(7) High level meetings took place on 17 January 2018, 22 March 2018, 8 June 2018, and 18 September 2018. Meetings at technical level took place on 24 January 2018, 6 March 2018, 22 March 2018 and 10 April 2018.

(8) As of the end of May 2018, the German authorities started providing first drafts of the documents describing the German companies' activities in the IPCEI Microelectronics. End of June 2018, the UK authorities provided first drafts of the documents describing the UK companies' activities in the IPCEI Microelectronics. End of July 2018, the Italian authorities submitted the documents for the Italian companies. At the beginning of July 2018, the French authorities started submitting the documents for the French companies. The Commission assessed the information in detail, in particular the eligibility and

[1] Microelectronics relates to the study and manufacture of very small electronic designs and components at micrometre-scale or smaller. These devices are made from semiconductor materials, and in particular the vast majority is made out of silicon.

[2] *[...] (*).*

**Confidential information*

compatibility of the IPCEI Microelectronics, the necessity of the aid, the research, development and innovation ("R&D&I") content of the research and development ("R&D") projects, R&D&I content of the first industrial deployment (also "FID") projects, end of the FID, eligible costs and funding gaps, spillovers and distortions of competition. To this end, the Commission assessed the submitted documents and requested further information in order to be able to carry out its assessment. The Member States complemented the information throughout August to November 2018.

(9) Germany, France, Italy, and the United Kingdom (hereinafter also collectively "the Member States") notified the abovementioned measures, respectively on 29 November (Italy) and 30 November (Germany, France and the UK) 2018. Further clarifications were requested by the Commission on 6 December 2018 and the German, French, Italian and UK authorities replied to such request on 6, 7 and 10 December 2018.

(10) By letters of 24 September 2018, the German and Italian authorities, and, by letter of 11 October 2018, the French authorities, respectively, agreed to waive their rights deriving from Article 342 of the Treaty on the Functioning of the European Union ("TFEU") in conjunction with Article 3 of Regulation No 1[3] and to have this Decision adopted and notified in English.

2. DESCRIPTION OF THE MEASURES

2.1. Objectives of the measures

2.1.1. Objectives of the IPCEI Microelectronics measures

(11) The Member States intend to grant aid to upstream microelectronic component manufacturers to carry out research, develop innovative technologies and carry out first industrial deployment in the EU, in order to enable research and development (R&D) on downstream microelectronics applications in two main markets, namely Automotive and Internet of Things[4] ("IoT"), as well as other important markets for Europe like space, avionics, and security.

(12) The Member States submit that the Important Project of Common European Interest on microelectronics "Connecting Europe's microelectronic industry to foster digitisation in Europe" [5] aims to develop a component offer that covers the full range of functionalities. The majority of electronic products must embed at least 3 or 4 different types of substrates, processes or components to gain their full functionality / autonomy / performances / cost affordability and create the systems required by markets.

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[3] Council Regulation No 1 determining the languages to be used by the European Economic Community (OJ 17, 6.10.1958, p. 385).

[4] The Internet of Things (IoT) is the network of devices, vehicles, and home appliances that contain electronics, software, actuators, and connectivity which allows these things to connect, interact and exchange data.

[5] Hereinafter referred to as "the IPCEI", or "the IPCEI Microelectronics" .

(13) The overall objective of the IPCEI Microelectronics project is to develop innovative microelectronics technology and components[6] for Automotive, IoT and other key applications and to establish first industrial deployment in these fields, in order to unlock the full technological and economic potential of the Key Enabling Technology ("KET") microelectronics and to transfer it to downstream industries for new or improved applications as well as new R&D in these sectors.

2.1.2. Contribution of the IPCEI Microelectronics to European Union's objectives

(14) The Member States submit that the IPCEI Microelectronics aims at contributing to the KETs[7] strategy and the microelectronics strategy[8], 'Europe 2020'[9], the 'Industrial policy'[10], and will enable value creation in downstream industries.

(15) Microelectronics has been identified by the Commission as one of the six KETs, crucial for the future development of European industry. As such, they are a priority for European industrial policy. The European Strategy for KETs aims to increase the exploitation of KETs in the EU and to stimulate growth and to create jobs. In its document "Europe 2020 strategy for smart, sustainable and inclusive growth"[11], the European Commission proposes a response to "Europe's innovation gap": "To boost future productivity and growth, it is critically important to generate breakthrough technologies and to translate them into innovations (new products, processes and services) that are taken up by the wider economy."

(16) In the Member States' view, the IPCEI Microelectronics directly supports these goals by providing the building blocks for new products and services which will become available and affordable for the population at large as the digitalization of society. Especially electronic components and systems contribute to the development of disruptive technologies across sectors, such as automotive and mobility (e.g. autonomous driving), energy (e.g. electricity management), and healthcare (e.g. remote monitoring). By enabling innovative solutions for societal needs and in the process of creating pan-European ecosystems along the value and supply chains, electronic components and systems are driving answers to respond to Europe's grand challenges.

(17) In addition, the purpose of the IPCEI Microelectronics is to foster cooperation in the large European ICT sector and especially across diverse IoT market segments. For this reason, the Member States consider that the proposed IPCEI is aligned with "Europe 2020"[12], the European Union's ten-year jobs and growth

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6 The specific details are described in sections 2.2. and 2.6. below

7 'A European strategy for Key Enabling Technologies — A bridge to growth and jobs', COM(2012) 341 final, 26.6.2012.

8 'A European Strategy for micro- and nanoelectronic components and systems', COM(2013) 298 final, 23.05.2013.

9 'Europe 2020, A strategy for smart, sustainable and inclusive growth', COM(2010) 2020 final, 3.3.2010.

10 'An Integrated Industrial Policy for the Globalisation Era — Putting Competitiveness and Sustainability as the Centre Stage', COM(2010) 614 final, 28.10.2012.

11 COM(2010) 2020 final, 3.3.2010.

12 COM(2010) 2020 final, 3.3.2010.

strategy, and Horizon 2020, "the main instrument for implementing Innovation Union, one of the most crucial initiatives of the Europe 2020 growth strategy."

(18) Microelectronics generates directly and indirectly employment all along the strategic European value chains, creating growth and wealth in the whole EU's economy. The Member States refer to the Commission Communication on the strategy for micro- and nanoelectronic components and systems.

2.1.3. Examples of downstream applications involved

(19) Further, the Member States point out some of the contributions of microelectronics on downstream applications:

- Microelectronics industry is a key contributor to EU's technology non-dependence in strategic domains with a clear reference to the emerging security issues. The European microelectronics industry allows to produce advanced critical devices to serve strategic sectors like transport, energy, health, finance, defence and space that have become increasingly dependent on network and information systems to run their core businesses. Europe has a need for a wide range of concrete measures that will further strengthen the EU's security capabilities in the microelectronics field, as a leverage effect to ensure that the EU is better prepared to face the ever-increasing security challenges.
- Europe's ability to innovate and improve its technology portfolio in all key industrial sectors depends on its ability to integrate high performance, low power and low cost semiconductor solutions in every single designed and manufactured product. For instance, with the onset of the automotive and IoT[13] networked economies, the need for a stable supply of trusted semiconductors is increasing even further. As the next wave of digitization is coming, existing European downstream value chains (automotive, industrial, aerospace, logistics, energy, lighting – as a few examples) need to explore the opportunities which will be enabled by advances in microelectronics. This is also a chance to create new value chains in the EU.
- In the near future in the automotive application domain, autonomous driving cars will require several components deriving from the IPCEI Microelectronics program and able to address two main challenges for the innovative cars: security and connectivity. The ultimate goal for a fully autonomous vehicle would be to dramatically cut the accidents rate, thanks to the electronics and software it will utilize. This will mainly happen due to large capacity of computation in real time, high speed/low consumption silicon chips but also dozens of cameras, detecting devices (radars, sensors, ...) to locate the car in its environment and alert on potential risks, and RF (radio frequency) components for the interaction of the car with other cars, the road infrastructure and various dedicated networks. The development of electric vehicles focuses on batteries, but also on the power semiconductor chips that will allow controlling the electricity flow between batteries and electrical motors on board.
- In addition, 5G, or the fifth generation of cellular technology, is characterized by its heightened speed, responsiveness and ability to handle

[13] For all acronyms, please see Annex 1.

a huge amount of connected devices. 5G could serve as the communications foundation for emerging technologies like autonomous driving, thus handling very sensitive data. Europe has to maintain its know-how for this potentially sensitive technology. As the risk of cyber-physical attacks is increasing, European industry as well as European citizens should be able to rely on the fact that neither their data nor the control of cars and machines can be improperly manipulated. Therefore, it has to be ensured that the microchips (and systems) cannot be influenced by external sources and that they offer enough security against all kinds of cyber-attacks, guaranteeing highest security and safety standards. The full control of this is only possible if security and safety are already built in into the chip design and are based on common understanding and standardisation. This requirement applies to all microelectronic components used in these emerging technologies.

(20) The Member States submit that the semiconductors are the components that are capable of producing such strong spillover effects, as the chips are an enabling key factor to provide technical solutions that address societal challenges or at least provide real-life applications for the users. The functionality of every single electronic device can be traced back to hardware (usually in conjunction with software). The versatility of microelectronics components makes this technology indispensable for every downstream market and across all industrial sectors.

2.2. Description of the IPCEI Microelectronics

(21) This section describes the IPCEI Microelectronics as it has been presented by the Member States in the notification.

(22) The IPCEI Microelectronics is organised along five technology fields (TFs):

- TF1: Energy efficient chips;
- TF2: Power semiconductors;
- TF3: Sensors;
- TF4: Advanced optical equipment; and
- TF5: Compound materials.

Within each of these fields, the participating undertakings will conduct both R&D&I and first industrial deployment (FID) activities.

(23) According to the Member States, FID in this IPCEI will allow for the development of new products with high research and innovation content and/or for the deployment of fundamentally innovative production processes. The success of the FID of a new technology and its related products will require a high level of integrated R&D&I on a continuous basis. The R&D&I efforts of industrial partners (within the FID phase) in collaboration with Research Organisations ("ROs") to achieve the FID will concern *inter alia*:

- the development of specific tools or methodologies,
- the collaboration within the whole European microelectronics ecosystem,
- the development of new technologies in close collaboration with dedicated suppliers (substrate, equipment, raw materials…),

- the development of platforms and open-access technologies.

(24) This IPCEI also comprises R&D works, focusing on:

- the development of new technologies for the next generation of devices, such as more energy efficient chips (along the More-Moore paradigm[14]), more powerful power devices, smarter sensors and faster bit rate communications,
- the adding of new functionalities to current devices (More-than-Moore paradigm[15]),
- the adaptation of current technologies to cope with emerging applications,
- the development of next generation products.

(25) These R&D works will result from close collaborations between the industrial partners, ROs and academic laboratories that are (or will be) involved in the IPCEI Microelectronics, as well as end-users.

(26) Such R&D works could also involve academic and industrial partners, which are not part of this IPCEI and which do not belong to any member state of this IPCEI, through European projects in the frame of the Eureka PENTA cluster or of the JU ECSEL. These collaborations will ensure the efficient dissemination of the results obtained within this IPCEI through the whole microelectronics ecosystem.

(27) Within each TF, a number of partners (participating companies) will join their efforts to address important challenges in the relevant field. The work in each TF will be organised in a number of work packages. The figure below summarizes the industrial partners and research organisations involved in each technology field of the IPCEI Microelectronics.

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[14] "More-Moore" corresponds to the miniaturization of the digital functions leading to electronic components benefiting from exponentially increasing computational power from one generation to the next.

[15] "More-than-Moore" refers to functional diversification of semiconductor-based devices. It complements digital signal and data processing in a product. These functions may imply among others analogue and mixed signal processing, the incorporation of passive components, high-voltage components, microsystems, sensors and actuators. "More-than-Moore" technologies allow non-digital functionalities to migrate from the system board-level into the package or onto the semiconductor chip. Technological progress from one technology generation to the other is not based on pure downscaling of structure widths on the semiconductor chip, but on optimizing a variety of parameters on the semiconductor chip as well as of the package design.

Figure 1: overall structure of the IPCEI Microelectronics

2.2.1. *Energy efficient chips (Technology Field 1, TF1)*

(28) In TF1, eight partners[16] in Europe will work to jointly address the challenge of improving the energy efficiency of basic microelectronic components, or chips. The participating entities aim to focused and aligned R&D&I for a qualitatively new class of products - energy efficient chips. The involved companies will continue by transferring these learnings into an FID phase. This, in turn, is expected to allow European companies to accelerate their R&D&I efforts leading to several significant benefits: the European R&D&I ecosystem along the entire value chain (upstream and downstream) to be strengthened, and innovative products and applications to be developed faster As a consequence, such strengthened European value chains are expected also much better to address a second big area of concern - the security at the chip or hardware level. The purpose of TF1, in order to contribute to the objectives of the IPCEI Microelectronics will be to develop, including in the FID, new, relevant, innovative, and energy-efficient techniques which will lead to new components to be incorporated in innovative end-products and applications in order to reverse the trend of ever higher power consumption by ICT/IoT in the future. So FID itself will lead to further R&D&I efforts in the TF1 community.

(29) The member states affirm that the participants in TF1 are jointly executing an important element of the European KET strategy in the field of Micro- and Nanoelectronics. Their focus is on advancing the energy efficiency of chips, a real challenge in light of the unprecedented proliferation of wired and wireless electronic devices connected with each other via the Internet. This challenge cannot be addressed by one entity alone regardless of its expertise in micro- and nanoelectronics. It takes close cooperation along the entire supply chain towards

[16] Considering separately ST – France and ST – Italy

the common objective of increasing the energy efficiency of microelectronic components, or chips.

(30) In order to facilitate and structure the cooperation within TF1, the work will be broken down into six major technical work packages ("WP"). Four of them are dedicated to technology development in line with the targeted application domains. Before first industrial deployment can occur, additional R&D activities have to be carried out such as meeting quality and reliability requirements as well as assuring manufacturability. These aspects are addressed in WP5. Another important aspect of the IPCEI Microelectronics is dissemination and spillover, and a specific WP6 is addressing that in order to maximize the impact of this project.

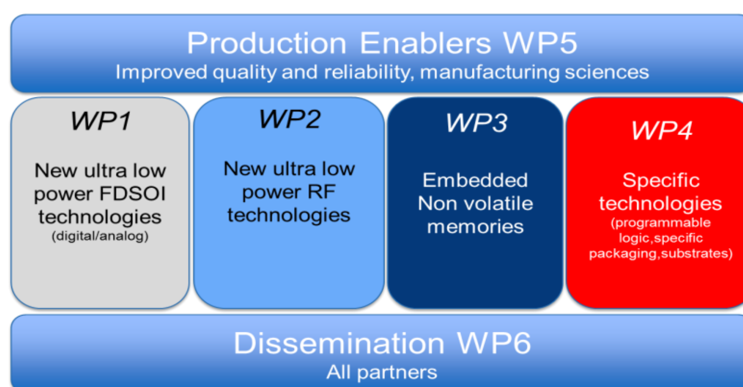

Figure 2: work packages in TF1

(31) **WP1 – New ultralow power FDSOI[17] technologies**. This part covers the FDSOI technology at the 28nm, 22nm and subsequent 12nm node. This energy-efficient technology is key in applications such as autonomous driving, computing, industrial, IoT, and aerospace, where computation capacity is required with a low power footprint. These technologies provide answers to the challenges brought by the various applications. In this domain, one of the objectives is to facilitate the FDSOI uptake by European industry in order to strengthen the upstream eco-system's innovation potential. Another objective to further close the gap between the digital and analogue realms. If signal or data processing is more and more digital, the interface with the real world is still analogue. As a consequence, there is a lot of demand for very efficient analogue technologies either as a dedicated one or as add-ons to the digital technologies in order to improve their performance in the analogue/mixed signal domain. The challenge is to develop highly performant European technologies which enable applications offering a real differentiation and combining the best from both digital and analogue domains.

[17] Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional bulk silicon substrates in semiconductor manufacturing. In Fully Depleted Silicon On Insulator (FDSOI) devices, the silicon surface layer is very thin so that the electrically-induced switching of electrons supports less interference resulting in higher switching speeds.

(32) **WP2 – New ultra-low power Radio Frequency (RF[18]) technologies**. The need for wireless communications is unlimited as it goes beyond connecting humans to connecting objects. It puts high pressure on RF technologies to keep up the pace of innovation. Switches, low-noise and power amplifiers, require improved figure of merit, that is, improved performance and/or efficiency of an innovative chip to address the new challenges posed by car-to-car and car-to-infrastructure communication, by proliferation of very low power communicating IoT devices, by e.g. low bandwidth IoT networks, and by 5G. The objective is to preserve the European position in communication by providing system makers with the best technologies to answer their new challenges in a most innovative and energy-efficient manner.

(33) **WP3 – Embedded non-volatile memory.** This is a very important technology especially for applications facing a very constrained energy budget such as IoT nodes. In this case, the major objective is to provide performant technologies which are able to support operations in a low power environment such as automotive or devices which need to function without batteries. This WP is targeting the development of various innovative flavours of embedded memories such as PCRAM, MRAM, and other R&D&I to FID activities.

(34) **WP4 – Specific technologies.** *[...]* One of the main objectives of WP4 is to provide tailored European technology solutions for fields such as IoT, Artificial Intelligence or space applications. The value stems from a strong and well-defined interaction between advanced wafer substrates, new chip designs and innovative semiconductor process technologies. *[...]*.

With the slowdown of Moore’s Law[19], the need for more integration of different functionalities on one chip and even more innovative packaging of one or more chips in one encasement is coming. This is driven by very specific conditions (such as in space) and by the need of integration of heterogeneous functions (such as digital, RF, and antennas). This WP is able to leverage the knowledge and technology present in Europe in order to provide new and innovative solutions for downstream users.

(35) **WP5 – Moving to FID.** This WP will address all the activities needed in a FID phase. To move an innovative technology from the stage of R&D&I to the subsequent FID stage requires a great deal of learning and continuous improvement efforts in terms of quality, reliability and manufacturability. Many sectors like medtech, automotive, security and aerospace for example have very stringent requirements on all of those dimensions. The required targets can only be met in a carefully planned and executed FID process.

(36) **WP6 – Dissemination.** Efforts will be undertaken to make the achievements of WP1 through WP5 available to a broad community of stakeholders including end users, large OEMs, SMEs and start-ups as well as ROs and academia.

[18] RF technologies are the different technologies involved in wireless communications, among others WiFi, mobile voice and data communications. They cover the wide radiofrequency spectrum from 3Hz to 3THz and the wide variety of technologies to generate and detect radiowaves.

[19] The exponential growth in computing power predicted by Moore's Law, named after Intel co-founder Gordon Moore, enables on a two-year cycle chips that are consistently more powerful than their predecessors even as the cost of that computing power falls.

Depending on the type of results, publications, technical events or commercially available IP will create an outreach far beyond the direct and extensive indirect scope of the IPCEI Microelectronics.

(37) The participating partners in TF1 will be Soitec, Globalfoundries, ST, X-Fab, Cologne Chip, Racyics and CEA-LETI.

The participating companies in this TF1 and their specific contribution will be the following:

(a) SOITEC (WP 1, 2, 4, 5 and 6): The FDSOI engineered substrates are the key to allow FDSOI technologies achieving industrial targets. The goal of the material specialist Soitec is to develop SOI substrates with high uniformity and low defect density and sufficient to enable foundries to ramp-up 28 nm, 22 nm, and 12 nm FDSOI technology node. The FDSOI innovation roadmap will be addressed in RD&I activity: it is aimed to provide SOI substrates with thinner buried oxide layers, so that the substrate will be the requirements of 12 nm technology node. Furthermore, new functionalities *[...]* will be added to current FDSOI substrate in order to increase their RF performance *[...]*. The targeted RF-SOI engineered substrates in 300 mm wafer diameter will bring cost and power effective approaches. Therefore, Soitec aims to develop 300 mm RF-SOI substrates which go well beyond the current state-of-the-art of 200 mm wafers. The RF-SOI innovation roadmap will also be addressed in R&D&I with the purpose to demonstrate RF-SOI engineered substrates with new materials enabling increased linearity performance and stability *[...]*. In addition, new Piezo-On-Insulator (POI) wafers *[...]* will be developed in the project. *[...]*. These activities of the partner Soitec will take place in new “Fab5G” line, Bernin 2 extension and Bernin 3.

(b) Globalfoundries’ (WP 1, 2, 3, 4, 5 and 6) goal in this project is the further development and establishment of the promising FDSOI technology. Therefore, the 22 nm technology node will be advanced in R&D&I activities and transferred to FID. In the FID phase, activities will be manifold process alignment and extended methods for process stability as well as the design for manufacturing and testing. It is aimed to enhance the diversity of FDSOI technology by using its outstanding properties (e.g. back-biasing) and thus, to develop a benchmark of new technology variants applicable for RF, mmWave and eNVM devices. With these devices, Globalfoundries targets to meet recent and future applications in IoT, consumer, and automotive. *[...]*. Finally, specific reliability for automotive applications will be demonstrated.

(c) ST (WP 1, 2, 3, 4, 5 and 6): The goal of ST is the development of a new generation of 28 nm FDSOI technology targeting low operating voltage for high-end and energy efficient microcontrollers. It is aimed to improve the RF capabilities of this technology as well as its robustness against harsh environments (e. g. in space applications). This also includes the introduction of dedicated FDSOI devices for high level hardware security in current and future nodes but also new packaging technology. Furthermore, it is aimed to research on high reliability and cost efficient process technologies based on Partial Depleted Silicon-on-Insulator

(PDSOI) to meet the requirements of low-power RF applications. In this context, ST will develop and evaluate novel dense eNVM cells in 40 nm technology node and novel Phase Change Materials in 28 nm technology node for their applicability in new non-volatile concepts. The overall target is to provide ultra-low power secure microcontrollers for automotive applications.

In particular, ST-France will be involved in developing and deploying ultra-low power FDSOI and RFSOI technologies, as well as new embedded non-volatile memories for MCU. Within this project some of its tasks will also concern the design of advanced devices based on these technologies.

ST- Italy will design and develop next generations of digital integrated circuits for microprocessors and ASICs, with specific critical safety functions like ADAS (Advanced Driver Assistance System) or autonomous driving and navigation.

Thus, planned RDI activities will cover the future devices for ADAS, 32-bit MCU (Micro-Controller Unit), and Telematics.

(d) X-FAB (WP 2, 4, 5 and 6) offers foundry services for processing analogue and mixed-signal semiconductor applications. In this project, X-FAB will develop chip level heterogeneous integration of different materials to improve the transmission and RF performance as well as functional reliability of novel energy efficient chips. In this context, enhanced SOI substrate materials offering high impedance will be developed. *[...]*. Furthermore, X-Fab will develop Process Design Kits with different level of maturity to demonstrate its technology to industrial partners.

(e) Racyics (WP 1, 2, 4 and 6) as an expert of designing analog, mixed-signal and digital integrated circuits (IC), targets on developing a versatile and energy efficient Multi-Processor System-on-Chip (MPSoC) platform for IoT applications. *[...]*. Furthermore, it is aimed to evolve IC design standards which meet the possibilities of the 22 nm FDSOI technology provided by Globalfoundries *[...]*.

(f) Cologne Chip (WP 1, 2, 4 and 6) as a developer and manufacturer of application-specific integrated circuit (ASIC) aims to develop and characterize novel structures and technologies for Field Programmable Gate Array (FPGA) applicable in 28 nm, 22 nm, and 12 nm FDSOI technologies. In this context, extensive investigations on timing and power extraction as well as modelling for integrated circuits required for industrial partners will be performed.

(g) CEA-LETI (WP 1, 2, 3, 4 and 6) aims to conduct fine analysis and develop an understanding of critical physical parameters and processing steps in order to develop future SOI substrates for the FDSOI technology. This includes the advancement of next structure generations of 12 nm and sub-12 nm width – in close cooperation with Soitec. Furthermore, in cooperation with the partner ST, CEA-LETI targets on the further diversification of 28 nm FDSOI technology node. In this context, novel

RF devices and functions based on this technology node as well as embedded Non-Volatile-Memories (eNVM) based on Phase Change Materials (PCM) are developed to be applicable in automotive and IoT. For completing the research portfolio, CEA-LETI will advance metal oxide based resistive Non-Volatile Memories (OxRAM), Magneto-resistive Random Access Memories (MRAM) as well as novel memory effect materials (e.g. Ferroelectric RAM) as potential alternatives. As a last goal, CEA-LETI will address silicon-based devices for quantum computing, neuromorphic architecture, and 3-dimenional monolithic integration to be able to offer technologies for future applications and the on-going digitalization.

(38) TF1 is necessary for the overall objective of the IPCEI Microelectronics because the urgency of improved energy efficiency and radiofrequency connectivity is cutting across all technology fields and downstream ICT markets and applications. The progress within TF1 will greatly contribute to the overall success of this IPCEI.

(39) According to the Member States, without the public funding provided within the frame of the IPCEI Microelectronics, R&D&I as well as R&D in FID efforts undertaken by the involved TF partners in the field of energy efficient and secure chips would be significantly lower in the European Union. This would deny the partners the opportunity to fully exploit the benefits of a technology whose time has come as application domains like IoT, Automotive, and Medtech etc. posing new challenges in terms of power foot-print and security. Eventually, the advances made possible by TF1, that is, the highly expected reduction of the carbon footprint from advanced electronic systems would not occur to the same extent. Specifically, without the aid to TF1, the consequences at technological level would be that the FDSOI and RF-SOI technology would not be further developed and the benefits in terms of energy efficiency and forthcoming 5G standards and components in Europe would not materialize. The partners in TF1 would resort to older, mature technologies. That would have a strong negative impact on the overall success chances of the IPCEI Microelectronics and its relevance for downstream markets like IoT which require more energy efficient solutions like the ones aimed at with the work within TF1.

2.2.2. Power semiconductors (Technology Field 2, TF2)

(40) In TF2, eleven partners[20] in Europe will cooperate to jointly address the challenge of power semiconductor devices with increased energy efficiency and reliability. Chip and package more and more merge and often chip and packages are only successful as a combined device where the chip and package are tailored to each other. The introduction of Industry 4.0[21] capabilities in the fabrication processes of these devices *[...]* will lead to more stable processes and thus improve reliability and robustness of the final semiconductor device. Robust devices have a higher durability, which reduces the electronic waste. The

[20] Considering ST – France and ST – Italy separately

[21] Industry 4.0 refers to the fourth industrial revolution corresponding to the current trend of automation and data exchange in manufacturing technologies. All objects (things) embark computing and sensing capacity are become connected in network to realise a truly intelligent system.

combination of power semiconductor devices with hardware based encryption (in a package or on a board) will enable critical infrastructures to be resilient against cyber-attacks.

(41) The goal of TF2 is to strengthen the European R&D&I in power semiconductors and integrated smart power solutions along the relevant value chain (chip technologies, assembly techniques, design/libraries, digital manufacturing, quality/reliability). The improvements along the value chain are a precondition for power semiconductors and integrated smart power circuitries of smaller size with less energy losses, with smaller cooling structures, with longer lifetime and meeting advanced application and market requirements.

(42) The respective contributions of the power semiconductor industry can be summarized in four major technical objectives:

- Sustainable energy generation and conversion,
- Reducing energy consumption,
- High reliability and functional safety enabled by embedded on-chip diagnostics,

(43) Efficient community energy management.According to the Member States, in order to structure the work within TF2, this technology field is organised in 5 work packages:

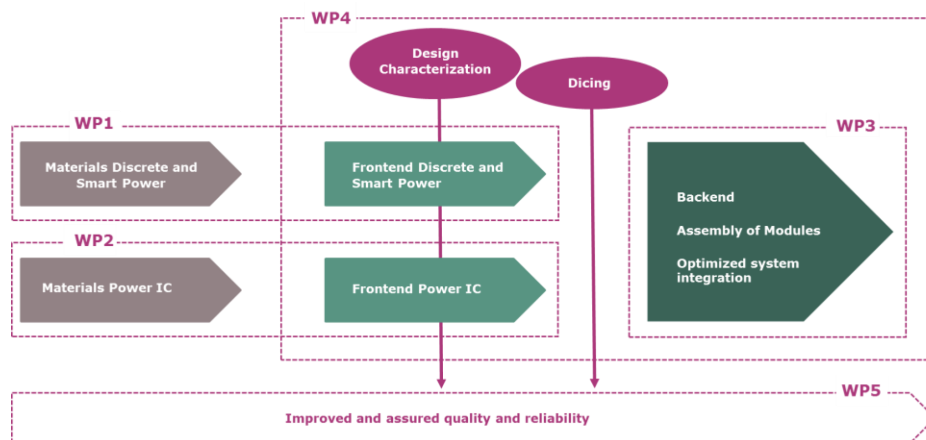

Figure 3: work packages in TF2

(44) **WP1 – New smart power and power discrete technologies**, with alternative materials (like GaN or SiC) as well as innovative combinations of different technologies, are mastering the more demanding market applications. Smart power technology integrates in the same chip different circuits having technological solution fulfilling different functions (analogue, logic and power). Such diversification allows approaching a wide range of application from automotive, industrial, healthcare, consumer, robotics, with the upmost goal to improve electronic systems efficiency and finally global CO_2 reduction. In addition, specific technological solutions allow improvement in terms of power density management simplifying package design and finally the product reliability. WP1 covers all essential aspects for the technology development (cost-efficiency, standards, test, etc.); including a variety of smart power process options and the critical process steps devoted to power discrete devices development. The variety of technology options will allow pushing forward the

new devices' innovation and differentiation. The WP1 goal is to push forward innovation in technologies, processes, and demonstrators and enhance the functionalities and performances of smart power devices according to the BCD technology roadmap (Bipolar CMOS DMOS (Double-Diffused Metal-Oxide-Semiconductor)) as well as of discrete power devices. The activities will be finalized to develop and validate new smart power devices and key process modules for discrete power devices on advanced technology platforms that will include smart power process technology node, featuring state of the art Power devices, high-density logic CMOS devices, high performance analogue devices and dense NVM architecture. Process development will be supported by advanced simulations for an effective design and by the processing of technology ramp up and monitor vehicles for reliability qualification and monitoring. The new technology platforms based on new alternative compound materials with SiC and GaN processes, will be the technological pillars featuring state of the art power devices, to address high performance devices with new architectures, and innovative modules for both diodes and discrete power devices.

(45) **WP2 – New High Voltage (HV) technologies for power integrated circuits** driving to better energy saving and efficiency improvement for automotive and industrial applications. Development of integrated power solutions for motor control and functional safe DC/DC applications using mixed technologies as the evolution of the smart power technologies from devices integrating a few power elements to a huge numbers of HV (*[...]*) drivers for medical or imaging applications. *[...]*. HV application are present not only in industrial and lighting market, but also in Automotive, where batteries pack involve some hundreds volts and galvanic solution represents the best approach. *[...]*.

(46) **WP3 – New assembly techniques** are related to the so called backend process of encasing dies (chips) in materials such as plastic, ceramics or metal. The objectives are to:

- Prevent the physical damage and corrosion of the semiconductor device,
- Support the electrical contacts to connect the smaller and thinner chips of the future to a circuit board,
- Dissipate heat produced in the device.

The work carried out under IPCEI Microelectronics includes development of new innovative package solutions with focus to enhance system integration. […].

(47) **WP4** – The focus of WP4 will be on development and implementation of **concepts according to Industry 4.0** to optimize the trade-off between flexibility and efficiency for the technologies worked out in WP1&2 (frontend related) and WP3 (assembly and packaging related). New automation concepts based on Industry 4.0 will ultimately lead to better quality of the devices made in Europe. For assembly and packaging, which supports system integration by multi-chip packaging, the work on Industry 4.0 (e.g. towards automation) is new in contrast to frontend technology. Thus, R&D&I in WP4 will strongly support the FID of the frontend related work in WP1 & 2 and the assembly and packaging related work in WP3.

(48) **Supporting WP5 – Improved and assured quality and reliability** during the implementation of new technologies.

The required specifications are measured at different stages of the fabrication process of semiconductor devices:

- Wafer test metrology equipment is used to verify that the wafers have not been damaged by the various processing steps up until testing,
- Once the front-end process has been completed, the semiconductor devices are subject to a variety of electrical tests to verify they function properly,
- The packaged chips are retested to ensure that they were not damaged during packaging and that the die-to-pin interconnect operation was performed correctly.

These are the first level reliability tests, i.e. tests that investigate just the packaged device. Thermal cycling and high temperature storage are examples of such tests. Moreover, second level reliability tests are required, which cover the application board, typically a printed circuit board. *[...]*.

(49) The contribution of the participating companies in this field will be:

(a) 3D-MICROMAC (WP 1, 2, 3, 4 and 5) will provide a new dicing technology which can be used for all types of wafers. More specifically, the work comprises of further development of TLS-Dicing™-technology and adoption to a broad range of power semiconductor products. Further development of microDICE™ machine technique with regard to requirements of the project partners as well as of additional potential European customers. 3D-Micromac will provide the technology to partners in form of a job shop model to support the development of new semiconductor products. Furthermore, 3D-Micromac will provide the technology in form of the „Pay-per-cut" model to selected partners at their own production site.

(b) AP&S INTERNATIONAL (WP 4) is a provider of equipment used for wafer wet-chemistry based processing technologies. The scope of work are development up to FID encompasses: the development of tools for wet-processes performed on wafers up to 300mm diameter and thinned to 40µm thickness substrates with highly-controlled process window options; the solutions developed use advanced robotics and new software features tailored to the scope of automation. Milestones have been defined for individual development packages used to develop, test and sample parts used by AP&S for the overall system design of the equipment.

(c) CEA-LETI will closely collaborate with Murata and ST in this project *[...]*. In this context, CEA-LETI and Murata aim to develop innovative dielectrics, new electrodes and associated process steps for advanced capacitors and show their performance in a technology demonstrator. Furthermore, CEA-LETI will conduct R&D&I activities on gallium nitride (GaN) power electronics and targets to meet the requirements giving by the partner ST.[…].

(d) ELMOS SEMICONDUCTOR's work (WP 2, 4 and 5) aims to R&D new HV technologies, developing manufacturing concepts up to FID to meet

high process quality and reliability. R&D&I will be carried out on the development of integrated power solutions for Motor Control and functional safe DC/DC applications using mixed technologies including assembly and packaging solutions, the development of corresponding strategies and solutions for failure analysis, reliability and test. Frontend-related work: HV mixed-signal CMOS technology; Backend-related work: R&D&I and FID for high parallel mixed-signal functional electrical test for power applications.

(e) INFINEON TECHNOLOGIES (WP 1. 2. 3. 4 and 5) aims to conduct research and development concerning both, frontend and backend-related technologies. This includes the frontend-related work of technology development of RF for power applications based on GaN (gallium nitrate). Backend-related work will relate to packaging of power devices *[...]*.

(f) MURATA (WP 1 and 4) is contributing innovative technologies for advanced passive components. This work addresses new smart power and power discrete technologies and developing and testing new concepts for manufacturing up to FID. Its frontend-related work will comprise of development of new advanced passive technology in order to be used in several applications compatible with the systems and technology (GaN, Si, etc.) developed by the IPCEI partners (incl. signal and power processing caps (high density, high breakdown voltage) and hybrid caps for energy management *[...]*. The company will also perform FID wafer fab line for innovative advanced passive technology.

(g) BOSCH (WP 1, 2, 4 and 5) aims to develop new techniques, which, thus, concern frontend-related work. This includes:

- Developing novel power technologies: Smart power in mixed signal technologies and high power discrete technologies with an emphasis on automotive applications will be advanced. *[...]*. These developments will be accompanied by the introduction of a series of innovations on the 3D integration and assembly, wafer thinning and high voltage isolation.
- Increasing substrate diameter: Parts of the R&D activities are carried out in the existing 150 mm and 200 mm process lines. The remaining R&D and FID activities will take place in a new 300 mm facility to be built.

(h) SEMIKRON (WP 1, 2, 3, 4 and 5) will perform mostly backend-related work: development of innovative processes for sinter interconnect and assembly with highest reliability and performance in power modules, the study of device reliability and ruggedness, the development of innovative fast test methods as well as the assembly of clean room power modules and systems with highest automation and quality standards; and cleanroom power module and system assembly line with highest automation and quality standards.

(i) ST Microelectronics France (WP 1, 2, 3, 4 and 5).

Frontend-related work:

- Power GaN device developments and First Industrial Deployment for power application
- *[...]*
- Advanced Silicon device developments and First Industrial Deployment for power and IoT applications

Backend-related work:

- Package solution developments and First Industrial Deployment for GaN device integrations for power application and space
- *[...]*

(j) ST Microelectronics Italy (WP 1, 2, 3, 4 and 5).

Frontend-related work:

- Power technologies (smart power technologies with differentiation in BCD (Bipolar CMOS DMOS) technology and power discrete technologies: *[...]*
- Production line ramp-up of "More than Moore" disruptive power technologies and first production parameters optimization

Backend-related work:

- New process technologies for System in Package mastering the big challenges in the packaging area

(k) X-FAB Germany (WP 1, 2, 4 and 5) aims to develop new techniques, which concern frontend-related work. This includes: development and FID of integrated High Voltage devices up to 700 V for modular integration in CMOS-based technologies and their demonstration in automotive, industrial and medical applications; R&D&I on GaN-on-Si technology modules in a CMOS-process environment. Furthermore, R&D&I activities on quality and reliability will be conducted: characterisation and modelling for robust and reliable power technologies including tests during FID; yield analysis and improvement for complex integrated smart power technologies; implementation of advanced process monitoring and advanced process control methodologies. During FID phase, X-FAB targets to develop new and advanced manufacturing concepts. In this context, real-time fab intelligence processes and other innovative fab logistic solutions for existing and new semiconductor processes and equipment will be developed and implemented. It is aimed to enable highly flexible manufacturing of small and medium production volumes up to FID of these techniques.

(50) According to the Member States, without the public funding provided within the frame of the IPCEI Microelectronics, R&D&I as well as R&D in FID efforts by the relevant industry in the field of power semiconductors would be significantly lower in the European Union and technological innovation as well as novel contributions to the value chain would not develop in the EU. The directly involved partners would not invest without the funding. This would lead to lower technological competences; the technological solutions on device security will not be developed to their full extent. The reduction of the carbon footprint from advanced systems would not take place to the same extent. Further progress in e-mobility would be delayed.

2.2.3. *Smart sensors (Technology Field 3, TF3)*

(51) The Member States submit that TF3 aims at enabling European sensor industry to develop and provide sensor components to the European market and thereby improving cooperation and R&D with respect to the European sensor industry. The twelve partners[22] of the TF3 cover the relevant value chain in Europe: sensors are at the core of most advances in the field of automotive electronics, IoT, including home and factory automation as well as health and well-being, authentication systems e.g. for security purposes, smart farming and efficient networks (communication, power, utilities) management in Europe. Smart sensors are also critical components in strategic segments such as aeronautics and space, which makes them a strategic asset.

(52) Sensors are the eyes and ears allowing controlling critical systems. They comprise optical, acoustic but also mechanical, magnetic, chemical, electrical and other types of sensors. They transform physical, real life information into a signal that can be used by electronic systems. Making sensors smarter is a necessity to reliably gather the right parameters resulting in processed and compressed data, which constitute the relevant information to be transmitted. Without mastering the right sensors and their integration the systems cannot become smart themselves. This is why the base elements developed in TF3 are becoming pervasive and are used in more and more applications.

(53) The Member States also point that another important aspect is to develop components for secure and trusted recording, transformation, transmission and processing of information. Complex systems with distributed intelligence, e.g. required for autonomous driving functions, need a comprehensive security architecture in order to prevent security violations. Smart sensors of the future will have increased signal classification and processing capabilities and consequently are the first line of defence against hacker attacks and security threats.

(54) Member States ascertain that would TF3 not be successful, the overall fields of security (biometric authentication is one example), industry and farming automation, automated driving as well as smart health care technologies would risk safety and security problems, delays and loss of relevance, or worse an uncertainty in the supply of critical components.

(55) The Member States submit that innovative sensors will be developed for various purposes by the partners of the IPCEI Microelectronics project towards first industrial deployment. The devices will achieve the full range of sensory functions to cover for the needs of Europe. The work in TF3 will be organised along the following work packages:

[22] Considering ST – France, ST – Italy, X-Fab France and X- Fab Germany separately

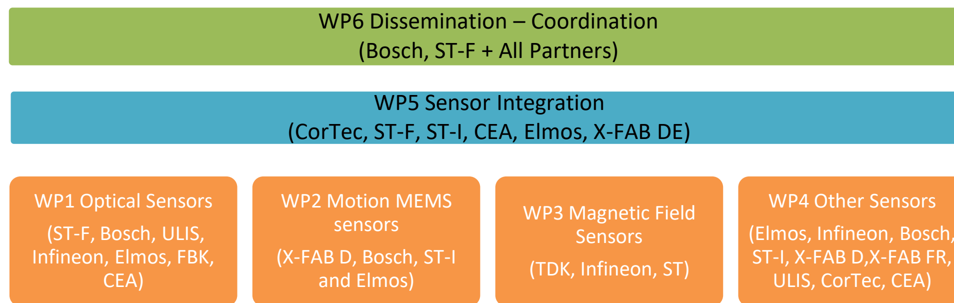

Figure 4: work packages in TF3

(56) **WP1 – Optical Sensors** (ST, Bosch, ULIS, Infineon, Elmos, FBK). A first important ability will be to perform object recognition by optical or alternate means – the eyes of a technical system. Optical sensors include image but also ranging sensors, ALS (ambient light sensors) and UV-index sensors, among others. *[...]*. Such different technologies permit to address the demanding needs of Automotive (Security, ADAS) and other growing sectors in Europe (Industry 4.0, Smart Cities, Wellness, AR).

(57) **WP2 – Motion MEMS sensors** (X-FAB DE, Bosch, ST-I, Elmos)**.** Motion MEMS sensors such as accelerometers and gyroscopes had the largest share of all MEMS produced since they are used in automotive (airbag, ESP...) and consumer electronics (switch portrait/landscape, gaming). They will continue to deliver an important contribution in the future as well. Therefore, several partners prepare first industrial deployment for sensors with novel approaches and applications. WP2 will work on a new technology for MEMS sensors improving sensitivity, resolution, bandwidth, and form factor to enable their usage for new application. *[...]*.

(58) **WP3 – Magnetic Field Sensors** (TDK, Infineon, ST, Elmos)**.** Owing to their various advantages like contactless sensing and high reliability, Hall sensors are indispensable components in the automotive and industrial sector. *[...]*. The next generation of sensors will outperform their predecessors' in different generic terms like sensitivity or signal to noise ratio, but also in further relevant characteristics like robustness and reliability (e.g. by stress-compensation or prevention technologies). Connectivity and smartness of such systems are also features, which are required by the "outer world" in which these sensors will be embedded and operated.

(59) **WP4 – Other sensors** (Elmos, Infineon, Bosch, ST-I, X-FAB DE, X-FAB FR, ULIS , CEA LETI, CorTec). In addition to optical and motion sensors, the expected sensory functions will leverage on / will be completed by the use of other physical sensors. They are piezoelectric, thermal, acoustic magnetic, or electrical sensors as an example, as well as temperature sensors and touch sensors, and more. In the framework of the IPCEI Microelectronics project, key involved project owners will aim to develop the next generation of these kinds of sensors for the targeted applications as automotive, IoT, health and others. *[...]*.

(60) **WP5 – Sensor Integration** (CorTec, ST, CEA-LETI, Elmos, X FAB DE)**.** All the different sensor types need to be integrated into a system in order to develop their full potential. This sensor integration is of crucial importance for the

performance of the final sensor system. The IPCEI partners within the TF3 will work on this sensor integration by preparing different technical solutions, which will provide several options to users and partners downstream the value chain for their specific final automotive or IoT systems. New System-in-Package solutions as well as new heterogeneous integration technologies to combine chips of different materials like micro-transfer printing will be investigated and developed in the TF3. Furthermore, the development and implementation of connection technologies like Through-Silicon-Vias to provide vertical electrical conductive connection through the silicon wafer are key to achieve at the end a 3D integration of different semiconductor components like MEMS sensors with CMOS integrated circuits with minimized footprint and height as required for mobile application for example. Novel soft (with silicone rubber) and hard (with ceramics) encapsulation technologies with high channel feed-throughs will be explored for providing sensors and systems for harsh environments.

(61) **WP6 – Coordination and Dissemination (all partners).** This work package contains the activities between partners involving cooperation within the technology field, participation to the overall governance of the IPCEI Microelectronics, and dissemination activities.

(62) The contribution of the individual partners in TF3 to the IPCEI Microelectronics project are the following:

(a) CEA-LETI (WP 1, 4, 5 and 6): together with ULIS, CEA LETI will work on a set of innovative technologies for Long Wavelength IR (LWIR) thermal sensors (so-called microbolometer). The aim is to establish brand-new thermal-based perception systems to Mobility (mainly Automotive) and Society (IoT) applications will work on enabling technologies and design for innovative CIS and Time-of-Flight devices, including pixel design, process steps, optics, 3D technologies, IPs and circuit design. In this context, the RO will closely work with ST as an RO, CEA LETI is only performing R&D&I activities (and as such no FID).

(b) CorTec (WP 4, 5 and 6) will establish a new cleanroom facility with dedicated and customized micro-machining equipment and complementary laboratories for R&D, usability and reliability investigations and testing to be able to develop innovative implantable MEMS-based sensor arrays and systems to enable electrical interaction with neural tissue for novel biomedical applications. CorTec's biomedical systems will use new chip technologies developed by other partners within IPCEI Microelectronics. Beyond the health applications, additional uses of the developed technologies will be explored in collaboration with the partners in this IPCEI Microelectronics (in all TFs) and with already established and new collaborations with European players outside of this IPCEI.

(c) Elmos (WP 1, 2, 4 and 6) aims to develop innovative mixed-signal (acoustic, optic, electromagnetic, thermal, pressure) sensor system solutions required for applications such as electric mobility, autonomous driving, smart home, smart car, medical applications, Industry 4.0 and security and start first industrial deployment. Additional R&D&I is planned along the sensor developments for needed functional testing, reliability and quality as well as assembly and packaging. Along with the

new sensor applications, strategic investments are necessary in sensor labs for R&D as well as sample and product verification, in new equipment for sensor processing and flexible test platforms allowing high parallel mixed-signal functional test. The further expansion of cleanroom capacities from previously unused space (in the Elmos fab in Dortmund) for laboratories and testing is planned.

(d) FBK (WP 1 and 6) will contribute to develop innovative Silicon Photomultipliers (SiPM) and Single Photon Avalanche Diodes (SPAD) with 3D integration. It will execute development and first industrial deployment of these optical sensors applicable for Automotive, health and IoT, and will enable technologies for 3D Integration and open platforms (PdK) for MPW (Multi-Project-Wafers). Therefor, FBK will develop novel technologies (e.g. Through Silicon Vias (TSV), Hybrid Bonding) for processing the envisaged high sensitive image sensors (SiPM and SPAD). It is aimed to integrate these technologies into a CMOS-like process and to provide 3-dimensional (3D) heterogeneous integration with deep-submicron CMOS readout electronics. The development of a reliable and reproducible process of TSV-SiPM will complete the project.

(e) Infineon (WP 1, 3, 4 and 6) aims to conduct R&D concerning both frontend and backend-related technologies. This includes the following work packages on frontend: sensor technology for radar applications (SiGe/Si-semiconductor technology), sensor technology for automotive applications based on magneto-resistive principles, sensor technology for mobile communication and Internet of Things. The work packages on backend will comprise of Fan-out Wafer Level Package technology (eWLB) for new applications in the field of sensors and flexible FID line for pressure and magnetic sensors.

(f) Bosch (WP 1, 2, 4 and 6) targets to research and develop highly innovative MEMS technology and smart sensors in cooperation with European partners within and beyond IPCEI Microelectronics. The focus hereby will be on applications in the automotive as well as the consumer domain. The RDI will address inertial and pressure sensors for consumer and automotive applications, as well as an optical micro mirror system for display. The particular challenge for the research and development of these devices is the further development of the MEMS element that needs to be strongly redesigned to reach the targeted high performances. Furthermore several innovations will be introduced through capacitive sensing and advanced packaging technologies. Another highlight is a new circuit concept for the evaluation electronics, which is trimmed for particularly low power consumption. These will result in innovative solutions, especially for new fields of application such as virtual reality (VR), AR, civil drones and indoor navigation. Unique semiconductor FID infrastructure and FID-equipment will be developed and implemented for 300 mm wafers as well as 200 mm wafers, setting new standards for automation. The goal is to introduce “digital factory” and Industry 4.0 principles as well as enforcing a flexible, adaptive and sustainable facility, in order to investigate the synergy and feasibility of combining, for the first time, mixed signal, power discrete processes and MEMS processes.

(g) ST-France (WP 1, 3, 5 and 6)

Innovative CIS, *[...]*

Time-of-Flight based innovative products, *[...]*

Enabling Technologies involving various bonding and multilayer approaches, and allowing new applications such as micro displays or optical free space communication

Innovative Integrated Vision Systems, involving inclusion of dedicated IPs

(h) ST-Italy (WP 2, 4, 5 and 6)

Work packages Frontend:

MEMS micro-actuators and intelligent devices technologies *[...]* for new MEMS in emerging applications

FID line enhancement for MEMS and smart sensors

AMR Magnetometer for E-compass applications (Location based services), Movement and Position detection as well as Magnetic field measurements (Magnetic Signature)

Work packages Backend:

New packing solutions to integrate the ASIC die & the MEMS sensors in a System in Package 3D configuration *[...]*

(i) TDK-Micronas (WP 3 and 6) aims to establish the next-generation of magnetic-field sensors within the IPCEI Microelectronics project. The well-known Hall Effect will be further utilized as the core technology for measuring the magnetic field through the introduction of a series of innovations to make such sensors much more sensitive, robust and integrated. This serves as an intermediate for many types of position sensing (linear, angle and 3D) in all kinds of application (e.g. Automotive, Consumer, Industrial). These new devices will set new standards with regards to performance and quality, as they will be more sensitive to the target and much more robust against disturbances like mechanical stress or external magnetic fields (e.g. EMC effects).

(j) ULIS (WP 1, 4 and 6) proposes to develop innovative thermal systems for emerging markets and applications where the thermal sensing will bring a clear added value in terms of performances, robustness and reliability. *[...]*. The ULIS project aims at developing a new range of technologies to enable the design and the manufacturing of new advanced thermal imagers dedicated to the Mobility, especially Automotive and IoT markets. *[...]*.

(k) X-FAB FR (WP 4 and 6) will develop an innovative open-access analogue mixed-signal technology platform suitable for the manufacturing of sensor ICs targeting multiple areas like automotive, industry, medical, IoT, and

others. The activities are mainly focused on integration of various functionalities like embedded automotive-qualified non-volatile memory, special optical sensing capabilities, etc. leading to a unique technology portfolio in Europe.

(l) X-FAB DE (WP 2, 4, 5 and 6) will focus on the development of next-generation MEMS-sensor technologies and special technologies for heterogeneous integration like micro-transfer printing to enable a new area of More-than-Moore technologies. New pressure and temperature sensor systems will be enabled by new wafer-level bonding technologies and special piezoelectric material integration and the capabilities of processing these sensor systems. The goal is to offer the necessary technology and standardized fully qualified open-access process blocks to serve different applications and to reduce time-to-market for end users. This will be supported by new to be established FID infrastructure which will apply Industry-4.0 concepts and will allow for new approaches regarding logistics and manufacturing execution.

(63) The Member States submit that without the public funding provided within the framework of the IPCEI Microelectronics, R&D&I as well as R&D in FID efforts done by the relevant industry in the field of smart and secure sensor systems would be significantly lower in the European Union. Technological innovation as well as novel contributions to the value chain would not develop in the EU. This would not only lead to lower technological competences of the participating partners. More importantly,

- the highly expected reduction of the carbon footprint from advanced systems would not take place to the same extent,
- the further development of the Industry 4.0 would be hindered,
- the further reduction of traffic fatalities would be slowed down, related to slower progress in automated driving.
- leading European OEMs of *[...]* systems for *[...]* and other applications will have to integrate sensors from suppliers who pose increased risk of *[...]* with respect to *[...]*.
- devices used in *[...]* and in *[...]* could be supplied by *[...]* fabs only to a lesser extent. *[...]* of the partners would be put into question.
- Increase of technical know-how by spillover effects by IPCEI Microelectronics would be stalled,
- Smart sensor networks will lay the technological base for new digital business models, since they serve as interface/link between the real world and its digital representation. Smart sensor may drive economy and society, on the precondition of leading edge sensor technology from the participating.

2.2.4. *Advanced optical equipment (Technology Field 4, TF4)*

(64) The Member States claim that the overarching objective of TF4 is to strengthen R&D&I for Europe’s semiconductor equipment industry with specific focus on Extreme Ultra Violet (EUV) technology, which is currently developed for introduction in the semiconductor factories for future high-end chip manufacturing in the next decade. To secure incessantly technical progress in

Europe, several technological challenges have to be met. Two of them will be addressed in TF4: the development of a EUV optics with sub-10nm resolution potential and the development of corresponding EUV masks, both in a performance meeting the requirements of future IC volume production. The EUV optical system to be developed is based on a new and totally disruptive technical approach never used for semiconductor manufacturing before. The same holds true for the EUV mask. Therefore the availability of both techniques might revolutionize the manufacturing process of integrated components and devices in future since it might allow improving the resolution of the patterning process of integrated circuits *[…]*. Fully exploring this resolution potential would allow decreasing the chip sizes of semiconductor integrated circuits *[…]*. Resulting from first R&D achievements, FID for the EUV optics systems and the EUV masks will be realised.

(65) In addition, the TF4 partners will develop Advanced Methods for Chip Manufacturing Enhancement and will make them available for all interested companies. This technique is still not in use at European semiconductor companies.

(66) The Member States submit that the work in TF4 will be organised in the following work packages, with contribution of the partners as described below:

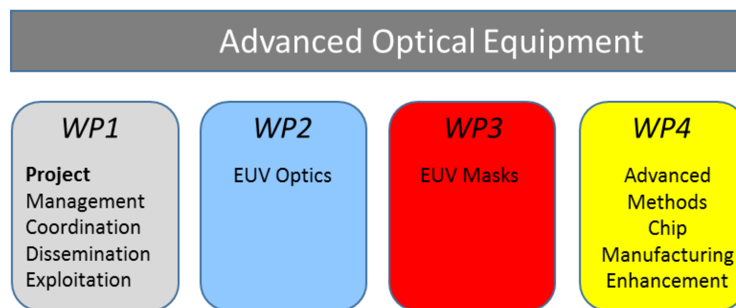

Figure 5: work packages in TF4

(67) **WP1 – Management.** (Lead Partner Zeiss) In this work package the development activities between the TF4 partners, and the collaboration with the associated partners will be coordinated. It supports the project leader for the timely supply of the project documents and the project reporting on technical results. It further organizes the exchange of results within the project, and the contributions to workshops and conferences for public dissemination. In addition, project engineering will be organized, specifically in case of deviations from work plans or adaption to a changing technical environment. Coordination towards the overall IPCEI Microelectronics project leader and governance organization will be done.

(68) **WP2 – EUV Optics.** (Lead Partner Zeiss): Development of a high resolution Hyper NA EUV optics system and corresponding manufacturing equipment for an optics factory

For high performing EUV optical system manufacturing about *[…]* tools and instruments need to be developed and installed in the optics factory, the majority of them will have to be tailored to the specific requirements for manufacturing of Hyper NA EUV projection systems. R&D&I activities will comprise in-house development and manufacturing of tools and instruments, enablement and

guidance of external suppliers, as well as activities needed for integrating the tools in the line and their technological process qualification. A variety of new unit manufacturing processes will be developed; most of them will by far exceed state-of-the-art technical manufacturing limits. At the end of the IPCEI Microelectronics project a line for fabrication of the optics components, modules and sub-systems and for their integration to the optical system will be available. All R&D&I activities will be based on preceding results for the Hyper NA EUV optics design, optics construction and integration concepts as well as advanced optics metrology concepts for both, the EUV projection objective and EUV illumination system.

(69) **WP3 – EUV Masks.** (Lead Partner AMTC) Development of a EUV mask manufacturing technology and first industrial deployment of a EUV mask manufacturing line.

A number of advanced tools will be implemented into the line, qualified and the associated unit processes developed to setup an integrated EUV mask line. These new tools address the critical unit processes of the mask manufacturing process and will enable with their advanced technology development of unit processes to achieve requirements of the Key Performance Indicators (KPI) of a EUV Mask.

The integration of a Multi-Ebeam-Writer as a complete new disruptive technology into the mask manufacturing process is pursued to enable required KPI on pattern placement and feature fidelity.

New etch tools will improve the uniformity of the features across the mask. High end inspection/repair tools will enable AMTC to find critical defects and improve mask defectivity to a level appropriate for a HVM chip manufacturing. R&D&I activities comprise the integration of the processes and their optimization to enable the needed mask quality capability. This includes also the determination of process limitations and the setup of procedures for process control. The development of a final mask manufacturing process requires deep understanding of the unit processes with the related evaluation and development steps and their interplay in an integrated environment.

In collaboration with AMTC, Zeiss will support the development of repair techniques for EUV masks, which can comprise chip layouts adapted to the Hyper NA imaging requirements. Such EUV masks will be indispensable for the success of future miniaturization of electronic devices based on EUV technologies.

(70) **WP4 – Advanced Methods for Chip Manufacturing Enhancement (AMCME)**

In WP4, joint R&D&I activities to develop Advanced Methods for Chip Manufacturing Enhancement with focus on logic devices will be carried out. The objective is to specifically improve the pattern CD control and overlay performance for logic devices, and by this contribute to improved manufacturing quality in semiconductor fabs. A partner within TF1 will apply the technique.

(71) The contribution of the individual partners in TF4 to the IPCEI Microelectronics project are the following:

(a) AMTC

The aim of the IPCEI Microelectronics project is to develop an EUV photomask line and to start the first industrial deployment of it to establish a novel and advanced EUV mask technology. To establish a line for EUV photomask targeting specifications for the 7 nm technology as next chip technology generation and below, novel manufacturing equipment with highly advanced capabilities are essential. Considerable R&D&I efforts have to be spent to bring these tools with the required specifications into AMTC's facilities. They need to be implemented before the mask process development with the relevant R&D&I efforts can be started.
The project includes the integration of *[...]* novel tools into the EUV photomask development line. Before, comprehensive equipment capability definition, a specification process and equipment evaluation is required, which often entails joint improvement projects with the tool suppliers and final process development utilising the novel tools.
Major R&D&I activities need to be spent for the mask manufacturing process development, which comprises - besides others - the introduction of new materials (e.g. resist or clean chemistry) and new processes to achieve optimum process parameters. Each single process has to be integrated into the overall EUV line process flow requiring additional R&D&I efforts. Due to its complexity, the interactions of the single process steps in the mask manufacturing flow have to be evaluated to identify crosstalk factors, and to finally achieve an integrated process meeting the intended tight mask specifications.

In all phases, AMTC will give feedback to tool supplier and joint R&D&I efforts will be made to improve all-over tool and process performance. In the FID phase, the EUV mask line will be optimized according to defect performance, yield and cycle time by development efforts on improvement of the unit process capability, and in particular on defect mitigation strategies and techniques to enable manufacturing of EUV mask with zero defects.

In collaboration with Zeiss, AMTC will develop special repair techniques for EUV masks, which will comprise chip layouts adapting the special Hyper NA EUV optics imaging requirements. In particular, AMTC will develop novel mask repair processes for different defect types and perform tests to verify the imaging performance as well as to stabilize repaired sites. Feedback will be given to Zeiss to improve their repair tool capability.

In addition, a development of Advanced Methods for Chip Manufacturing Enhancement with focus on logic devices will be carried out. The objective is to specifically improve the pattern CD control and overlay performance for logic devices, and by this contribute to improved manufacturing quality in semiconductor fabs.

Together with Zeiss, AMTC will test and improve the methodology from a view of a mask maker, starting with defining specification and conducting of tests on special test masks.

(b) Zeiss

Zeiss will develop a highly innovative, disruptive optical system for manufacturing of integrated semiconductor components and devices: *[...]*. The imaging technique to be developed will require a totally new optical concept, which is based on using only mirrors as imaging components instead of glass lenses and *[...]* to achieve the required magnification in both image field coordinates. Furthermore, Zeiss will progress the manufacturing base for the corresponding EUV projection optics towards FID. More than *[...]* tools and instruments for manufacturing of the optical system will be developed. Most of the equipment has to achieve technical specifications, which will approach the limits of what is feasible within the laws of physics and make this project truly an undertaking of major innovative nature.

For repair of advanced EUV masks, Zeiss will transfer EUV application specific know-how of its repair and inspection equipment to AMTC. Technical equipment advances worked out in running ECSEL projects during the IPCEI Microelectronics time frame will be made available to AMTC to ensure, that reliable mask repair processes will be available in time.

Another objective of Zeiss is - together with its TF4 partner AMTC - to develop AMCME and to make this innovative technique introduced first time in Europe for logic IC manufacturing. It has high potential to improve the functional performance of ICs, the chip manufacturing yield and Cost-of-Ownership (COO) significantly through improvement of feature line-width and overlay control.

(72) The Member States claim that without the public funding provided to the TF4 within the frame of the IPCEI Microelectronics, the companies' R&D&I budget and CAPEX originally planned for the project period (2018 to 2020) will be stretched by at least *[...]*. As a consequence, the delivery of first prototypes of EUV optics systems and EUV photomasks will be postponed to *[...]*. As a consequence the first full volume production ready EUV optics and EUV mask delivery would shift to *[...]*. A late market availability will significantly increase the EUV technology market entry risk.. Moreover, a delay of the IC miniaturisation speed would result in a slowing technical progress, higher costs per electronics product and/or a reduced technical performance with negative consequences on all industrial sectors in which electronics is a key enabler.

2.2.5. Compound materials (Technology Field 5, TF5)

(73) The Member States submit that the overarching objective of this technology field is to create an integrated, pan-European, compound semiconductor ecosystem, with the following targets:

(a) Increase in Compound Semiconductor (CS) technologies which will enable and support TF1-4 and other technological areas, across the supply-chain.

(b) Engage downstream organisations to create a strong user community which will pull through the CS technology developments to enhance applications.

(74) Ten partners will work together to create an end-to-end supply chain of compound materials and devices, used across multiple applications. The

increasing demands of power consumption across the Internet within sensing and telecommunications, requires devices which are faster, more energy efficient, cheaper and of higher capacity. TF5 will strengthen the relationship along the supply-chain, through collaboration within IPCEI Microelectronics between partners from materials and equipment through to device fabrication, packaging and end-use application. It will use cooperation partners from outside the IPCEI Microelectronics within academia, ROs and SMEs in order to perform design, process development and prototyping. All the outputs expected from the IPCEI Microelectronics project are typical indicators of key enabling technologies addressing the megatrends towards miniaturization and the convergence of photonics, electronics and microelectronics.

(75) The work in this TF will be organised in the following work packages:

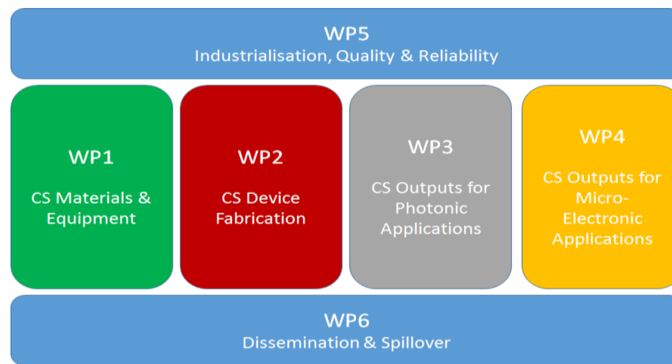

Figure 6: work packages in TF5

(76) **WP1 – CS materials and equipment** (IQE, AZUR SPACE, OSRAM, Soitec, SPTS, ICS, CEA-LETI, Sofradir)

This work package concerns the development, as well as the installation, commissioning of equipment to manufacture CS materials. In the main this will involve, but not exclusively, epitaxial wafers (epi-wafers) of III-V, II-VI and IV-IV semiconductors grown to partners' specifications for feeding into WP2, 3 and 4. The most prevalent materials will be based on GaAs, InP and GaN. In addition, it will involve the manufacture of special substrate materials and also equipment for wafer processing. All aspects such as facility build, equipment installation and commissioning, process and technology development and ramp-up towards first industrial deployment will be involved. Other aspects will be „open-access" epiwafer capabilities using novel engagement models that will be developed during the project, potentially also in conjunction with WP6. The technology development will build on R&D&I prior to IPCEI Microelectronics in underlying projects from previous collaborations. The major goal of this WP in IPCEI Microelectronics will be to grow materials beyond the state-of-the-art to larger diameters, on novel substrate materials and with higher throughput towards first industrial deployment – with a view to a large equivalent-area cost-reduction, whilst maintaining performance.

(77) **WP2 – CS device fabrication** (NWF, OSRAM, ICS, AZUR SPACE, ST-F, CEA-LETI, Sofradir)

This work package will develop devices based on materials obtained from WP1, and potentially from other sources outside of the project. There will also be

aspects of equipment installation and commissioning to process the CS materials. It will also therefore include process and technology development and ramp-up towards FID. Processing lines will be developed, or modified to provide FID for ever-larger epiwafer diameters. *[...]*. In addition, the possibility of „open-access“ device fabrication capabilities will become highly probable, again potentially using novel engagement models developed during the project and in conjunction with WP6.

(78) **WP3 – CS outputs for photonic applications** (OSRAM, AZUR SPACE, ST-F, ICS, NWF, CEA LETI, Sofradir)

This work package will focus on developing photonics-based outputs with targeted applications in telecom, sensing and energy efficiency for end-use in e.g. Internet of Things, lighting, automotive (e.g. LIDAR, interior displays), data-centres/fibre-to-the-premises and aerospace and security, etc. It will develop outputs from WP1/WP2 across the following fields; miniaturized and micro-LEDs will be developed for advanced lighting, AR/VR and projection requirements; *[...]*. There is also considerable potential for „cross-over“ with TF3 (sensors) where material and devices manufactured in WP1 and 2 may be designed and tested.

(79) **WP4 – CS outputs for microelectronic applications** (AZUR SPACE, ST-F, ICS)

This work package will focus on developing micro-electronics based outputs with targeted applications in energy efficiency applications. It will also develop outputs from WP1 and WP2 across mainly power applications using novel materials such as GaN and SiC. To this end, there will also be considerable potential for „cross-over“ with TF2 (power electronics) where material and devices manufactured in WP1 and 2 may be designed/tested/qualified with those partners in that TF.

(80) **WP5 – FID quality and reliability** (All partners)

This work package will focus on aspects required to take the processes in WP1-4 through the learning phase towards FID covering issues such as reliability, reproducibility, quality control and standardisation. This will also include improvement towards Industry 4.0 practices and also adaptability and agility in the approach to new technologies and their deployment.

(81) **WP6 – Dissemination & Spillover** (All partners)

This work package will ensure that, along with the other TFs, the results of the IPCEI Microelectronics project are disseminated to the wider audience – to partners outside of IPCEI Microelectronics and to those outside the technologies and countries within the project. It will do so through the normal routes, such as key international conferences. In addition, it will also plan events such as workshops and seminars, designed to „educate“ those not yet familiar with the TF.

(82) The specific contributions of the partners in TF5 will be as follows:

(a) Sofradir will innovate through two key projects: *[...]*.

For the *[...]* project the work plan under IPCEI Microelectronics will be broken down into: definition and installation of the pilot line for large dimension wafer processing; large dimension wafer growth and process development; large Focal Plane Array (FPA) development, prototyping and test; definition, installation and test of the FID tools. For the *[...]* project the work will consist in: material and performance modelling; pilot line definition and installation; technology development; high-operating temperature FPA development, prototyping and test; definition, installation and test of the first industrial deployment tools.

(b) ST intends to develop and put in FID next generation photonics devices and BiCMOS for multiple applications including datacom, telecom, automotive, 5G. ST France activities will expand from *[...]*, to BiCMOS with the development and FID of a high performance and low cost integration platform.

(c) AZUR Space aims to realize both, optoelectronic components (disruptive, patented monolithically stacked photodiodes and laser power converters) and power electronic components *[...]*. Therefore, running R&D work with external partners is continued (funded 100 % by AZUR SPACE), epitaxy equipment for Metal-Organic Vapour Phase Epitaxy (MOVPE) will be installed in existing buildings *[...]*, processing equipment (for opto and power partly in common) and characterization tools (opto and power) will be commissioned, installed, put into operation and ramped-up.

(d) OSRAM aims to explore and develop smart and highly integrated optoelectronic components and devices with novel functionalities. Within this work package, materials and devices and the required highly complex processes for such outputs will be developed and their transfer towards a more scalable production environment will be explored. Five major sub tasks are planned for future product lines: chip scale package: highly compact white emitting LED devices with minimum of package material, scalable over more than an order of magnitude in size (side length of chip/device); miniaturized RGB LED arrays as the building blocks for narrow pixel pitch video walls providing ultimate resolution and large scalability of brightness, e.g. for sunlit outdoor applications; smart pixelated LEDs, wafer- and chip-level integration of pixelated LEDs and CMOS for ultra-compact monocolour and white emitting arrays, e.g. for automotive and general lighting; UV and deep UV LEDs, high power and reliable LEDs *[...]* for industrial applications *[...]*; integrated 200mm GaN-on-Sapphire first industrial deployment, a first fully integrated processing line for 200mm wafer supply of the entire value chain (epitaxy, chip, dicing, converter deposition and packaging).

(e) IQE: the company is specialist for development and fabrication of compound semiconductor epiwafers, which are the essential base for all CS micro-electronic and photonic devices. This will include the development of new compound semiconductor crystal growth technologies on larger wafer diameters for the 4 types of targeted wafers, the development of process control innovations to reach the challenging wafer uniformities in thickness, composition and doping, as well as the development of structural and functional characterisation techniques. The

partner aims to provide unique and high IP compound semiconductor epitaxy wafers by further developing epitaxial deposition processes: establishing *[...]* laser epitaxy; establishing *[...]* laser epitaxy; establishing *[...]* Epitaxy for Power Electronics; establish *[...]* Epitaxy. Furthermore, it aims at MOCVD Equipment installation and commissioning together with required metrology; test and characterization against benchmark wafers and from iterative partner feedback; preparation for scalable prototyping of larger diameter epitaxy; cross machine yield and uniformity analysis, release from RDI to first industrial deployment and to complete full integrated yield management (IYM) high throughput and reproducibility analysis.

(f) Newport Wafer Fab: the company, as a chip foundry, will be using the internal TR Advanced Quality planning process for R&D and FID for photonics. NWF will further bring innovation in process technology by the development of deep trench etching with advanced chemistries to pass through various materials in a single process. It will also introduce and develop a fast-cycle electron beam lithography for photonic component fabrication. As Photonics partner it will: provide photonic designs and system applications know-how and will work with major end user OEMs towards their future commercialisation. As LED partner it will: install, commission and establish LED equipment set at 200mm, with back end equipment and metrology including test and measurement; establish integrated yield management (IYM) across process flow and back end packaging; sign off and release to first industrial deployment; transfer standard LED modules and full process flow; Test LED flow with benchmarked samples; transfer micro LED flow - test and benchmark against early 150mm prototypes for arrays; Sign off power LED process flow for limited FID.

(g) ICS : it will focus on: commissioning and build of a new *[...]* cleanroom for first industrial deployment, including test and qualification areas; procurement of all required frontend and backend equipment for wafer and die level processing; hiring, training and qualification of new personnel; increased fabrication process reliability and FID stability including quality improvement of discrete detector outputs, ramping towards first industrial deployment levels; prototyping of integrated detector outputs; development of high data-rate integrated detectors including low noise APDs and monolithic integration of passive components on InP APD chips combined with novel bandwidth enhancement techniques for substantial enhancement of component performance. Use of multi-pass optical techniques for substantial enhancement of component performance; qualification of integrated detector outputs on new first industrial deployment infrastructure.

(h) SPTS: will research and develop deep trench etch process and equipment *[...]*. The following work will be executed during the project: (1) dicing for Power, MEMS and CS – plasma dicing and pre/post integration, including Concept & Feasibility (C&F) investigations into plasma dicing of compound, MEMS and Power substrates, Beta system development and deployment of compound, MEMS and Power substrates, C&F investigations into opening of dicing lanes (pre plasma dicing) using laser

grooving and other technologies, C&F investigations into singulation post plasma dicing of die with backside coatings, Beta system development and deployment for pre-plasma dicing and post-plasma dicing; (2) piezoelectric materials – deposition and etch technologies, including Beta system development/deployment of deposition for next generation MEMS/RF filters, Beta system development/deployment of etch systems for next generation MEMS and RF filters; and (3) Compound Semiconductors, including hardware and process development for advanced compound semiconductor manufacture, deployment of these technologies into the Compound Semiconductor Cluster environments.

(i) Soitec will develop innovative Compound Semiconductors dedicated to micro-LEDs and advanced photonics as well as SOI platforms for Silicon photonics, from R&D to first industrial deployment. The following tasks will be executed during the project: Task 1 Micro-LEDs: development and FID of a disruptive substrate (InGaN-on-Sapphire) that will enable the fabrication of efficient red, green and blue micro-LEDs on the same starting material. This innovation is expected by the emerging market of microdisplays for AR glasses, pico-projectors, head-up systems for cars and aeronautics. Task 2 Photonics: development and FID of Silicon-On-Insulator (SOI) substrates allowing unprecedented performance gain and extending the SOI Photonics roadmap. Also, develop layer transfer of InP-on-Silicon as a low cost solution for Silicon photonics integration.

(83) CEA-LETI is partnering with Soitec, Sofradir and ST-Microelectronics. With Soitec, CEA-LETI is collaborating on new materials developments for LEDs and photonics through material growth and technology. With ST, CEA-LETI is working on photonics technologies *[...]*, especially through modules and IPs design, 3D and other enabling technologies, process steps. CEA-LETI is also working with ST on SOI CMOS technologies *[...]*. With Sofradir, CEA-LETI is working on high performance infrared detectors through development in the fields of materials, device design, semiconductor processing, packaging and test. CEA-LETI will also participate in the prototyping phase of the detectors.

(84) The Member States submit that without the public funding provided within the framework of the IPCEI Microelectronics, R&D&I as well as R&D&I in FID done by the relevant industry in the field of compound semiconductor materials would be significantly lower in the European Union and technological innovation as well as novel contributions to the value chain would not develop in the EU. Several activities and developments for new applications in e.g. automotive and IoT will not be realized at all with strong consequences on technological availability and employment in Europe. This would lead to lower technological competences in Europe. This will also have a strong impact on *[...]* aspects coming into focus the global digitalization. Furthermore, the reduction of the carbon footprint from advanced systems would not take place to the same extent.

2.3. Governance of the project on Microelectronics

(85) The Member States submit that the governance of the IPCEI Microelectronics will supervise, monitor and assure the implementation of the IPCEI microelectronics at large. This especially concerns the monitoring of the implementation progress of individual partners as well as the consortium as a

whole. The focus of the implementation is on both, technological advances as well as the spillover activities to disseminate these advances, which the individual beneficiaries have committed themselves.

(86) The governance will be performed by the Supervisory Board (SB) incorporating
- the Public Authority Board (PAB), with representatives of the Member States participating in the IPCEI Microelectronics;
- a representative of the European Commission; and
- the IPCEI Microelectronics Facilitation Group (FG).

(87) At least once a year, the IPCEI Microelectronics General Assembly gathering all IPCEI Microelectronics beneficiaries, the funding authorities of the IPCEI Microelectronics Member States and the European Commission will be organized.

(88) While the members of the PAB and the EC guest will be appointed by the Member States and the European Commission respectively, the members of the FG will be elected by the representatives of the IPCEI Microelectronics General Assembly.

(89) The IPCEI Microelectronics FG shall be composed of
- A chair and the deputy for the overall IPCEI Microelectronics project;
- The coordinators of the five technology fields and their substitutes; and
- Additional company representatives to assure a balanced contribution of large and SME companies. At least 2 members of the FG have to be representatives of SME.

(90) At the first IPCEI Microelectronics General Assembly (*[…]* after approval of the European Commission) the members of the three Supervisory Board bodies shall be nominated officially. The General Assembly is an internal meeting for the IPCEI Microelectronics participants only, but it shall be organized alongside the annual public IPCEI Microelectronics conference (see below) in order to combine the efforts of attendance with dissemination and spillover activities.

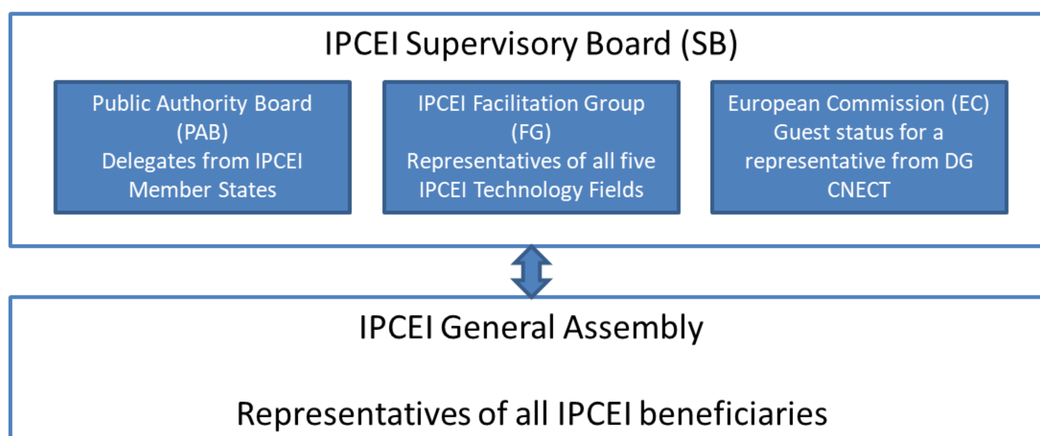

Figure 7: IPCEI Microelectronics Governance structure (as submitted by the Member states)

(91) The FG will be in charge to organize SB meetings which will be held twice a year. One SB meeting will be held in the frame of the European Forum for Electronic Components and Systems (EFECS), the second one in the middle of

the year at changing locations where spillover activities will take place in non-participating countries at the same time.

(92) Furthermore, the FG will drive the overall progress of the technology fields on a non-confidential basis to permanently interface with private and public stakeholders with the goal to highlight the IPCEI Microelectronics' role and impact via annual execution reports (based on reports from all five technology fields), publications and conferences in Europe. To demonstrate the effectiveness of the IPCEI Microelectronics setting and functioning, Key Performance Indicators will be agreed upon at the first meeting of the SB and monitored accordingly in the course of the project.

(93) The role of the Technology Field Coordinators (TFC) will be to organize the collaboration within their TF. Regular meetings, at least once a year as part of the IPCEI Microelectronics General Assembly, are devoted to present and monitor the progress of each of the five technology fields. The TFCs are obliged to prepare a yearly summary report on the progress and the results in their respective TF. These reports will focus on technological advancements as well as the spillover activities to which the members of the TF have committed themselves. This report will be complementary to the individual reports which will have to be delivered by each partner to the respective national funding authorities.

(94) The FG will also be responsible to organize and foster the collaboration and the communication within the project and to third parties which can benefit from the IPCEI Microelectronics results but are not partners in the project. For this, effectively two instruments will be implemented by the FG: 1) The annual IPCEI Microelectronics conference, 2) the IPCEI Microelectronics website.

(95) The annual IPCEI Microelectronics conference will be devoted to inform the interested expert community on the R&D-progress and the technical results of the IPCEI Microelectronics. The IPCEI Microelectronics conferences will be associated to the European Forum for Electronic Components and Systems (EFECS) that takes place annually in autumn (usually Nov.) at different locations in Europe. The EFECS is the largest conference for innovation in Microelectronics in Europe.

(96) The central IPCEI Microelectronics website will be set-up shortly after the notification. It will foresee a restricted area for IPCEI Microelectronics participants only in order to organise the implementation of the project.

(97) At the same time, the website will host public information about the project and all involved partners. Moreover, the website will serve as the dissemination and interaction channel of the IPCEI Microelectronics project to engage with non-IPCEI Microelectronics organisations. For this, the website will list all spillover activities to which the individual IPCEI partners have committed themselves and that are addressed to interested European organisations and companies outside the IPCEI Microelectronics. This information will be presented in form of an "Events Calendar" with the concrete dates and a brief description of the activity. The interested community will have the opportunity to register for participation at the activities directly with the IPCEI partner who is in charge of the specific activity, being it a roadshow, a hackathon or any other activity as committed by the individual partners. The website thus also will also serve as a

basis for the annual reporting on the delivery of the committed activities. The FG will collect qualitative and quantitative information for each activity, i.e. who participated with which feedback and the immediate impact of the participation. The FG will aggregate this information within the annual progress reports and by this demonstrates the spillover impact of the IPCEI Microelectronics as a whole.

(98) The Member States have confirmed that the national funding authorities are in possession of the commitments of all IPCEI partners. As such, the PAB will be responsible to monitor the completeness of the listings and announcements of the committed spillover activities.

2.4. Integrated project

(99) The Member States submit that the IPCEI Microelectronics is an integrated project within the meaning of point 13 of the IPCEI Communication[23] in light of the elements described in this section 2.4.

(100) In order to take the opportunity represented by the proximity of the European microelectronic ecosystem with other industries, this IPCEI Microelectronics project aims to involve all the microelectronic capabilities in Europe to meet and coordinate these needs.

(101) The scope and technical, scientific and innovative coverage of the project led the national authorities to support the project as an IPCEI Microelectronics according to a construction that allows to pool risks. In addition, the project involves partners from all the Member States promoting the project and involves a very large part of the European ecosystem linked to the microelectronic sector.

(102) The governing rules defined by the Member States allow a coordinated follow-up of the implementation and execution of the work at each stage. An evaluation of the work is carried out in stages to redirect them in the event of disruption or to cease financing in the event of technical failure of the project.

(103) Because of its breadth and level of scientific and technological complexity, the IPCEI Microelectronics requires a large number of partners to work together on alternative technologies. There has to be an intensive and interdisciplinary collaboration and close coordination. The results obtained by a partner will impact the work of the others.

(104) The IPCEI Microelectronics project is organised along technology fields and the coherence of the project is evidenced by the inter-relations of them. The technology fields are not only complementary; they are mutually connected and

[23] "The Commission may also consider eligible an 'integrated project', that is to say, a group of single projects inserted in a common structure, roadmap or programme aiming at the same objective and based on a coherent systemic approach. The individual components of the integrated project may relate to separate levels of the supply chain but must be complementary and necessary for the achievement of the important European objective" – p.13 of COMMUNICATION FROM THE COMMISSION Criteria for the analysis of the compatibility with the internal market of State aid to promote the execution of important projects of common European interest, published in OJ 2014/C 188/02 of 20.06.2014 (hereinafter referred to as "IPCEI Communication").

depend on each other. Typically, markets do not demand single component or chips, but systems based on a combination of elements developed in and delivered by different fields. Nevertheless, the parameters of this digital revolution involve technological and economic challenges to the microelectronic sector:

- the integration of the cooperating down-stream partner needs before the development of a new technology, even in the first step of the technology fields (substrate, production equipment);
- the economic model based on the deployment of heterogeneous components for small and medium volumes;
- the development of specific components integrating all available functionalities.

(105) More precisely, the interlinks and relations between the technology fields, which are aimed at the common objective and are based on a coherent systemic approach, are as follows:

2.4.1. Integration of TF1 within the framework of the IPCEI Microelectronics

(106) Work within TF1 enables energy efficient and RF technologies for data processing, data collection and data communication in electronic systems which also include power devices (from TF2), sensors (from TF3), lithography equipment enhancements (from TF 4) and compound semiconductors esp. in the case of data centers (from TF5). In particular, the electrification of mobility and further digitization of production as well as products and services (best summarized as Industry 4.0 and IoT) require the interplay of Power Semiconductors and integrated Smart Power circuitries from TF2 with the energy efficient and RF components from TF1. Energy efficient and RF technologies are indispensable for the take-off of IoT.

(107) Furthermore, the sensor technology developed in TF3 relies heavily on the component technologies from TF1. Always-on sensor solutions with wake-up systems required in embedded applications and particularly autonomous driving are for example made possible with ultra-low power FDSOI technologies. These sensors from TF 3 will also need ultra-integrated and low power SOI based RF Front End Modules from TF1 for 5G compatibility.

(108) In addition, TF1 process technologies will also benefit from the equipment progress made in TF4. It is foreseen that the to-be-developed Advanced Methods for Chip Manufacturing Enhancement (AMCME) will be applied in first trial runs with a TF1 partner for the purpose of developing advanced logic devices.

(109) Finally, on the topic of autonomous driving and *[...]*, TF1 has common fields of innovation and optimization with TF2 and TF5 respectively. In the case of the latter, increased cooperation between TF1 and TF5 actors will address the issue of energy efficiency *[...]*. Relationships between TF 1 and 5 are further strengthened as the respective activities contribute to the convergence of photonics, electronics and microelectronics in a wide range of IoT and other applications.

(110) TF1 is necessary for the overall objective of the IPCEI Microelectronics because the urgency of improved energy efficiency and Radiofrequency (RF) connectivity is cutting across all technology fields and downstream ICT markets and applications. The progress within TF1 will greatly contribute to the overall success of this IPCEI.

2.4.2. Integration of TF2 within the framework of the IPCEI Microelectronics

(111) Smart applications in the fields of IoT, Industry 4.0 or mobility require the interplay of power semiconductors and integrated smart power circuitries from TF2 with the energy efficient and RF components from TF1. Especially for integrated smart power circuitries the connectivity for data exchange between systems will be an aspect becoming more and more important. The technologies of TF1 are the base for important components in smart power systems by providing the necessary performance for data communication.

(112) Mutual synergies between TF2 and TF3 will be created. Special (integrated) *[...]* devices and components developed in TF2 will be used for certain sensor applications where electric power needs to be efficiently coupled to enable the operation of sensors. Furthermore, special manufacturing topics addressed in TF2, like flexible manufacturing of *[...]*, will be used and applied for activities in TF3 as well. Sensors developed in TF3 can be of great use in the FID phase for TF2. Inertial or optical sensors can be used on equipment for TF2 to detect *[...]*.

(113) The work conducted within TF2 on compound semiconductors will benefit from synergies with TF5 (Compound Semiconductors). The overlap between the TFs is demonstrated by the same epitaxial processes for Gallium Nitride (GaN) on Si and on SiC. For instance, *[...]* is offering epitaxy to *[...]*.

2.4.3. Integration of TF3 within the framework of the IPCEI Microelectronics

(114) Smart sensors play a crucial role in the integrated IPCEI Microelectronics project among the project partners and technology fields. Smart sensors are semiconductor and microtechnology based and integrated in sensor systems including components and technologies developed in the other TFs. Due to this, strong interaction with the other TFs synergies and enabling technologies will be leveraged in the IPCEI Microelectronics to develop a strong European ecosystem and *[...]* in the area of Smart Sensors. Since Smart Sensors are used to continuously monitor the environment or status of machines, cars, industrial systems etc. the energy-efficient technologies developed in TF1 are a crucial contribution to these sensor systems in order to enable a very low energy consumption during operation and even energy-autonomous sensing. Furthermore, TF1 develops technologies for wireless communication of the sensor system as it is important for many applications like IoT. TF1 results in efficient processing and storage will fit in new smart integrated sensors *[...]*.

(115) Special (integrated) *[...]* devices and components developed in TF2 will be used for certain sensor applications where electric power needs to be efficiently coupled to enable the operation of sensors. Furthermore, special manufacturing topics addressed in TF2, *[...]*, will be used and applied for activities in TF3 as well. The same is true of for the improvement of processes based on results of

TF4. An important aspect of smart sensors is the heterogeneous integration of these sensors with other silicon components *[...]*. TF5 is dealing with such materials applicable for smart sensors *[...]*. Another example of TF5 and TF3 relationship is the introduction of light sources, lasers or light emitting diodes, which are developed using compound semiconductor materials and are combined with optical sensors to achieve a complete function *[...]*. TF3 will develop up to first industrial deployment technologies enabling smart sensor and system integration related to the other TFs.

(116) TF3 will contribute to the other technology fields in several ways. Many of the integrated circuits developed in TF1 being related to sensor integration or sensor signal processing, the knowledge of the new developments in the sensor fields will allow to develop better and efficient integrated circuits and technologies. Also, *[...]* sensors, and *[...]* solutions proposed in TF3 will be combined with the concept of "energy efficient chips". The same is valid for TF2 related to power. Intelligent powering systems need to take into account the characteristics of the sensors they are developed for. Moreover, TF3 will deliver sensing elements into TF2 that add evaluation circuitry to form a complete microsystem. Specifically for TF5, photonics sensors as well as microelectromechanical systems (MEMS) actuators are used for the integration of the systems in communication equipment, *[...]*. For TF4, the high precision optical manufacturing relies on the best sensors and often distributed sensors. *[...]*.

2.4.4. Integration of TF4 within the framework of the IPCEI Microelectronics

(117) Beyond strengthen the European semiconductor equipment manufacturing sector by new Research and Development (R&D) achievements and FID activities for EUV optics and masks, the partners of the TF4 will also contribute to an increase of the R&D&I expertise of the microelectronics sector in Europe. Therefore, in a first phase, collaboration with a partner of TF1 is planned to develop Advanced Methods for Chip Manufacturing Enhancement (AMCME). This *[...]* approach *[...]* will be developed and tested at first with this TF1 partner specifically for the development and FID of logic devices. Zeiss and AMTC together with the TF1 partner will develop the technological basics for using this technique at logic chips. Based on the technical achievements, this technique can be transferred also to other IPCEI partners of TF1, TF2 and TF3, and other interested companies not involved in the IPCEI Microelectronics. AMCME will provide manufacturing excellence advantages wherever *[...]* are decisive parameters for the performance and the yield of electronic components.

2.4.5. Integration of TF5 within the framework of the IPCEI Microelectronics

(118) To achieve the goals within the IPCEI Microelectronics, strong European partnership is required to develop a core competence across many of the technologies in the Micro- and nanoelectronics and Photonics KETs. To drive further energy efficiencies and develop sensor technologies, TF5 will be positioned to develop novel CS materials technologies into several other TFs.

(119) New materials such as GaN and SiC will find ever-increasing roles in Power Semiconductor technologies and TF5 will offer several collaborative opportunities in this regard with TF2. This is exemplified in the similar epitaxial capabilities of *[...]* being developed by both technology fields.

(120) New sensing applications such as LIDAR in automotive and gas/chemical environmental monitoring and other photonics-based devices will offer further collaboration with TF3. In addition, energy efficiency requirements e.g. within data-centres, can be enabled by CS-based devices and will be targeted for increased cooperation with TF1.

(121) As with many semiconductor processes, CS materials are very dependent on Equipment, in order to ensure that the metrology and fabrication of both epiwafers and devices respectively, will be performed using the most state-of-the-art tools in order to meet partners' specification requirements. In the case of epiwafers, optical, structural and electrical characteristics need to be verified in order to conform to requirements, whilst these wafers will be processed through fabrication lines using evaporation, deposition, etch and lithography tools, such as those developed in TF4, in order to fabricate devices. There will be considerable scope for cooperation between those epiwafer and device fabrication partners in TF5 and the new technologies being developed in TF4.

2.4.6. *Collaboration within the IPCEI Microelectronics with respect to the technology fields*

(122) In addition to the inter-relations of the technology fields, strong collaboration of the IPCEI partners within and across the technology fields will exist. There will be more than 110 collaborations within IPCEI Microelectronics of which at least 44% would not occur without IPCEI Microelectronics.

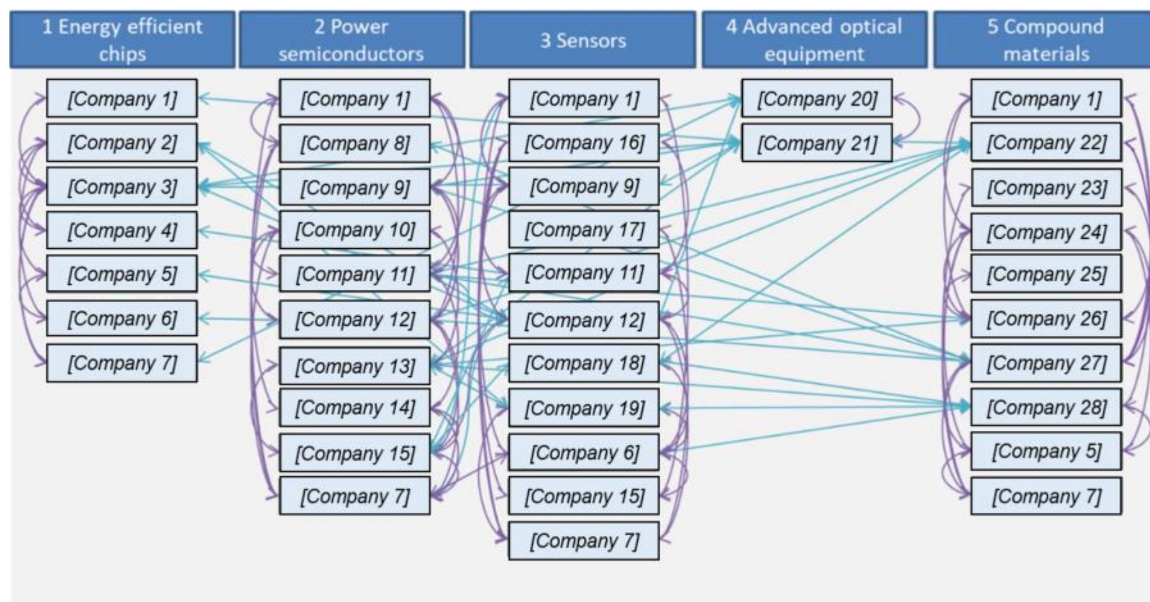

Figure 8: Collaborations within IPCEI Microelectronics with respect to technology fields

2.4.7. *Examples of joint contribution by the TFs in downstream applications*

(123) The Member States have stressed that the smart phone is a good example of the integrated nature of the IPCEI Microelectronics across its five technology fields. The Member States point out that practically all communication chips for current and future generations contain a combination of compound semiconductor and silicon chips. Furthermore, there are a variety of smart sensors in the phone ranging from gyroscope and accelerometer, to range

finding sensors for camera autofocus, pressure sensors, proximity sensors and many other smart sensor chips. Finally, there are several power management chips required to switch voltages and to minimise the power consumption of the phone.

(124) Another example of integration can be evidenced in the automotive sector. Automated driving cars will require to tackle two main challenges: security and connectivity, the ultimate goal being the fully autonomous vehicle that will dramatically cut the accidents rate, thanks to the electronics and software it will utilize. This will happen thanks to large capacity of computation in real time, thanks to high speed/low consumption silicon chips but also dozens of cameras, detecting devices (radars, etc.) to locate the car in its environment and alert on potential risks, and finally RF components for the interaction of the car with other cars, the road infrastructure and various dedicated networks.

(125) And while the development of Electrical Vehicles (EV) will mainly focus on batteries, it will also require power semiconductor chips that will allow control of the electricity flow between batteries and electrical motors on board, and fast charging.

2.5. Positive spillover effects generated by the project

(126) The Member States confirm that the wide spectrum of R&D&I activities within the IPCEI Microelectronics project, ranging from industrial research to FID, will produce positive spillover effects in form of new knowledge, networking and cooperation opportunities, which reach far beyond the core partners and participating Member States addressing the microelectronics sector and other industrial sectors throughout the European Union. The project's work will result in technological advances of a generic nature. These advances may ultimately benefit products and application areas other than those initially targeted. This new knowledge and know-how will be widely disseminated through various channels described below.

(127) They submit the following concrete and detailed examples of spillover and dissemination for the benefit of European economy at large, not limited to the IPCEI Microelectronics consortium nor to the participating Member States. According to the Member States, these examples are representative but non exhaustive of the IPCEI Microelectronics potential, since new, other spillover and dissemination will likely develop during or after the project.

2.5.1. Dissemination and spillover events

(128) The Member States point out that much of the knowledge generated and transmitted by IPCEI partners will be made accessible to the entire semiconductor industry via technical conferences and publications. For example, scientific personnel of ROs and enterprises will present the newest R&D results at these conferences and publish these R&D results in peer-reviewed, scientific journals. For example, procedures and methodologies for robust sensor design or guidelines for the qualification of high performance consumer components for automotive or industrial applications can be used by system companies all over Europe. Relevant information and results will be shared with the public at specific IPCEI Microelectronics events as well as at a

number of well-established international conferences. IPCEI partners will contribute to the most relevant events regularly (see Table 1).

Name of event/conference	**Description**
EFECS, European Forum for Electronic Components and Systems	The annual conferences address key strategic challenges facing the Electronic Components and Systems value chain. Breakout sessions will explore the Strategic Research Agenda and the technology roadmap for Europe as well as address societal needs.
SEMICON Europa	The annual SEMICON Europa is the venue for meeting and exploring low / high power and high Radio Frequency applications, as well as manufacturing solutions for flexible, hybrid and highly integrated electronics.
EPOSS (European Technology Platform on Smart Systems Integration) Various events per year	Within EPOSS, a group of major industrial companies and research organizations from more than 20 European Member States intend to co-ordinate their activities in Smart Systems Integration.
ESSDERC and ESSCIRC	The annual *ESSDERC and ESSCIRC* events will provide a European forum for the presentation and discussion of recent advances in solid-state devices and circuits with respect to the increasing level of integration for system-on-chip design.
ESREF – European Symposium on Reliability of Electron Devices, Failure Physics and Analysis	This annual symposium focuses on the latest research developments and future directions in failure analysis, quality and reliability of materials, devices and circuits for micro-, opto-, power and space electronics.
EMLC – European Mask and Lithography Conference	Annual conference
Compound Semiconductor International Conference	A 2-day conference attracting more than 550 European delegates connecting, informing and inspiring the compound semiconductor industry detailing breakthroughs in device technology; insights into the current status and the evolution of compound semiconductor devices; and advances in tools and processes that will drive up fab yields and throughputs

Table 1: Selection of important international conferences for dissemination

(129) The 29 partners of the IPCEI Microelectronics will publish themselves some of their R&D results in the various international scientific journals, and will present their results on numerous conferences. In addition, a large part of the software tools will be developed under an open source license and will be widely disseminated[24].

[24] The Member States draw attention to the fact that such ways of knowledge dissemination was validated by the Commission in its decision on N437/2008 –Nano 2012 and in its decision on SA.37747 (2013/N) - Nano2017.

(130) Roadshows and workshops will be organized to spillover IPCEI related knowledge and innovations to companies and particularly to SME's in Europe.

(131) Moreover, dedicated IPCEI Microelectronics events will be organized by the IPCEI Microelectronics Facilitation Group. The R&D-progress as well as the technical results of the IPCEI Microelectronics project will be disseminated regularly at a conference in the frame of the EFECS which annually takes place in autumn (usually Nov.) at different locations in Europe. On this IPCEI Microelectronics conference the partners are committed to report the progress on their technologies in the frame of IPCEI Microelectronics with regard to existing and new application areas. The first IPCEI Microelectronics conference will be held during the EFECS 2019 (19.-21.11., Finland). Further examples of events organized by the Facilitation Group are a General IPCEI Microelectronics Convention, to be organized twice each year, which will inform about IPCEI Microelectronics progresses and will favour further networking with non-IPCEI companies and ROs, and specialized workshop on specific IPCEI topics (e.g. ultra-low consumption sensors, new compounds substrates, new equipment) with two types of events: scientific presentations and round tables, in order to create occasion for both the academia and the industry.

(132) All these events will be geographically distributed in order to reach as many EU Member States as possible, covering both Member States that participate and Member States that do not participate in this IPCEI. Besides events, dissemination will be organized by web communication, web-sites and social media. There will be an official IPCEI Microelectronics website that will contain all important information about the project, the technological news, and the partners for those European (EU) large enterprises, SMEs, and ROs which are interested in benefiting from the IPCEI Microelectronics and coming in contact with consortium partners. This webpage will be installed short-term after the start of the project, probably in the first quarter of 2019.

2.5.2. Dissemination to the European collaborative R&D&I ecosystem

(133) The Member States submit that the IPCEI Microelectronics project has a very large collaborative R&D&I part which combines, beyond the strict scope of notification, no less than 223 partner and research organizations active in 16 EU Member States.

(134) The IPCEI partners will collaborate in particular in European collaborative research programs under the PENTA and ECSEL programs and the Framework Program for Research and Technological Development (FP RTD; Horizon 2020 and FP9 from 2020). The partners in these projects will conduct research complementary to that carried out in the IPCEI Microelectronics; their contributions will draw heavily on knowledge and expertise developed in the IPCEI Microelectronics.

(135) The research areas covered by the FP9 are at the heart of the ECSEL technology roadmaps, which are jointly established by all European players in the sector. This European collaborative framework enables a large number of partners in the European Union to share methods and results on a specific technological issue.

(136) Another important European framework, also involving some of the IPCEI partners, is the European Institute of Innovation and Technology (EIT), with active participation of Italy in the Knowledge Innovation Communities (KICs), that have been launched in Europe as the EIT-Digital (FBK and ST Italy are active partners) and the EIT-Raw Material KICs.

(137) In addition, the European Strategy Forum on Research Infrastructures (ESFRI) EuroNanoLab involving multi KET (mKET) research infrastructures provides important support to mKET companies.

(138) The Member States provide the following examples for collaborations between IPCEI partners in some of the described frameworks:

- X-FAB is already coordinating two ECSEL pilot line projects (ADMONT, MICROPRINCE) related to the technology fields of power semiconductor and sensors with in total 26 partners from nine different EU Member States.
- *[...]*.
- *[...]*.
- *[...]*.
- *[...]*.

(139) The Member States claim that the aid to the IPCEI Microelectronics will make it possible to significantly increase the level of knowledge dissemination, only by increasing the number of academic partners directly and indirectly involved in the project.

(140) The work of the academic partners will focus on the development of scientific models and technological bricks, with specific skills identified according to the targeted themes. The results obtained by these partners will also have a markedly generic character: for instance, they could be used for a large number of different new integrated circuit designs and production. These advances may also benefit products and application areas other than those initially targeted in the project. Because of their marked generic character, the knowledge developed by the academic partners of the project will be difficult to appropriate.

(141) In addition, the academic partners of the project will have full latitude to disseminate results that do not give rise to intellectual property rights, through scientific publications, papers in conferences, etc. On the Crolles and Grenoble sites alone, there are more than *[...]* publications (referenced journals and conferences) per year. By estimating that industry and academics will also publish without involving the IPCEI partners, the Member States estimated that more than *[...]* publications could be produced during the project. The IPCEI Microelectronics will also likely lead to a large number of doctoral theses and post-doctoral periods, the results of which will be widely disseminated. It is estimated that *[...]* approximately *[...]* theses can be started in relation to the IPCEI Microelectronics.

(142) Member States claim that the outcome between research and industrial partners of these projects is a valuable input for the IPCEI Microelectronics project. The IPCEI Microelectronics results will trigger additional collaborative R&D&I projects with research and industrial partners. In addition, new technological

challenges will trigger close collaboration between research partners inside and outside the IPCEI Microelectronics.

(143) Another key element in the dissemination of knowledge is the access given to *[...]* installed on the premises of IPCEI partners. Microelectronics research requires validation of the work carried out on batches manufactured under real conditions. Academic research in microelectronic technology is therefore only possible to the extent that it can be based on pilot R&D equipment, the cost of which is prohibitive for the academic world. This reasoning also applies to SMEs.

(144) According to the Member States, these close links between the IPCEI Microelectronics and the European collaborative research programs will therefore contribute to the wide dissemination of the knowledge and know-how developed to other European research laboratories and industrial partners

(145) In the absence of support for the IPCEI Microelectronics, not only the dissemination of knowledge gained from this major project via European programs would be lost, but also the ability of these programs to rely on competent actors to develop the ambitious technological roadmaps that motivated their implementation. In fact, in the absence of a permanent and sufficient training effect, it is the maintenance of the capacity to develop advanced device technologies in Europe that could be challenged.

2.5.3. Dissemination of IP unprotected and protected results

(146) The Member States confirm that results, which are not subject to registered and unregistered Intellectual Property ("IP"), will be widely and freely disseminated in technical and scientific publications and theses. They however note that some of the publications relating to the work of the IPCEI Microelectronics will follow the filing of patents or other protected intellectual property rights.

2.5.4. Dissemination by exploiting the use of the IPCEI Microelectronics results outside the targeted sector

(147) The Member States submit that open-access foundries, *[...]* offer semiconductor manufacturing technologies to companies without having own IC or MEMS products on the market. All open platform technologies can be used for a wide variety of applications by other companies. Therefore, foundries are not limited to a certain application or market and all R&D&I activities have a huge leverage effect for the business and economy in general. In addition, all released technologies can be used independently from the required manufacturing volume. By this especially SMEs are enabled to use state-of-the-art semiconductor technologies for their products.

(148) In particular the foundries can participate to this European ecosystem with multi-project wafer (MPW) capability, free process design kit (PDK) access. This open-access foundry business model is well suited to delivering spillover for the IPCEI Microelectronics project into the wider European community. *[...]*.

(149) The Member states claim that technologies, process and products developed in this IPCEI Microelectronics have a great potential for unpredicted and wide spillover as such, and provide for the following examples: accelerometer sensors that were initially invented to trigger the deployment of the airbags in a crash are today used in smartphones. This usage of the sensor could not have been foreseen initially. It is expected that the technologies invented during this IPCEI Microelectronics will have a wide spillover to other markets. Another example of spillover beyond the targeted sector is shown by *[...]*. *[...]*. Co-development for agricultural or industrial monitoring, *[...]* answer key societal challenges.

(150) They also support that the strong expertise and results generated within the IPCEI Microelectronics will be the main pillar to facilitate the support for the creation of new start-ups in different technical domains and related applications, to be considered also "outside IPCEI Microelectronics main areas of interest".

(151) The technology developed during IPCEI Microelectronics will contribute to important development in other application areas which are of interest for the EU as a whole, such as:

- Body monitoring
- Air and water quality
- Food quality and composition – allergy related monitoring by sensors for fast detecting of allergenic or bacterial components – (e.g. Photonics applied to health) EU FP7-Symphony project – Integrated system based on PHOtonic Microresonators and Microfluidic Components for rapid detection of toxins in milk and dairy products).
- Agri-Food: The microelectronics technologies development will boost new applications and use IoT solutions in the Agri-Food domain (sensors and traceability for precision farming and agro-logistic, increased food quality level and awareness, etc.), enabling a huge number of SMEs throughout Europe.
- Cultural Heritage: The needs of preservation, security and fruition specifically related to this application domain, can largely benefit from the technical results and innovative solutions coming from microelectronics. RFID (Radio Frequency Identification) tag can enable identification, fruition, traceability of the artworks; inertial and magnetic sensors, can also allow the real-time location of single objects, monitoring shock protection for a safe transport and display.

2.5.5. Dissemination through standardisation activities

(152) The Member States ascertain that standardization is an important factor for dissemination and is a sound way to propagate and ensure the high visibility of the project results across related communities. Providing new products and processes should bring new standards for future technologies.

(153) Standards are essential in building ecosystems with wide participation. Standards also foster collaboration, they help to reduce development times, and impact the cost of product ownership. As such, all products in compliance to generally accepted standards can generate return faster, reach higher peak volumes and are easy to service or replace by similar products. The generation of standards creates a spillover effect to companies along the value chain enabling sensor and component manufacturer, system integrators and OEMs to

develop their products with drastically reduced time to market and high market acceptance.

(154) The IPCEI industrial partners are present in several standardization bodies and consortia with different roles (founder, member, etc.) in technical and management committee. The objective of these activities is to contribute technical expertise for choosing the most innovative solutions and to advise on the feasibility of implementations in order to improve the overall quality of relevant standards. The participations include among others:

- https://www.airfuel.org/ – Airfuel Alliance develops new wireless charging standards, comprised of two of the most advanced wireless power technologies-inductive and resonant charging;
- https://www.wirelesspowerconsortium.com/ – Wireless Power Consortium is an open-membership organization to promote the adoption of a global standard for wireless charging, named Qi;
- https://openconnectivity.org/ – Open Connectivity Foundation is a consortium devoted to new specifications to unlock the massive opportunity in the IoT market;
- http://www.ieee.org/ – IEEE the Institute of Electrical and Electronics Engineers;
- http://www.aecouncil.com/ – Automotive Electronics Council component technical committee is the standardisation body for establishing standards for reliable, high quality electronic components;
- http://www.semi.org –- SEMI brings together industry experts through a number of committees to develop global accepted technical standards;
- https://www.eusemiconductors.eu/esia/home – EECA/ESIA is the organization representing the European semiconductor industry in Brussels;
- http://www.aeit.it/ecsel/struttura/pagedin.php?web=ecsel&cod=home – ECSEL Italia, supports the interest of Italian firms and national public research centres, active in the sectors interested in enabling technologies of electronics and intelligent systems, with regard to the Joint Technology Initiative (JTI) ECSEL (Electronic Components and Systems for European Leadership), launched by the European Commission.

(155) *[...]*.

(156) The Member States claim that the vision of IPCEI Microelectronics is pushing the standardization[25] of the main developed technologies (across the whole value chain) and it will have a direct implication for lowering the barrier of adoption. With a rich variety of skills and activities in the IPCEI Microelectronics, the involved partners comprise huge expertise coming from different domains and standardization committees and are committed to proactively reduce barriers for technology and market penetration. By taking part in technical standardization bodies, the IPCEI partners can support them with industry experts in order to facilitate globally accepted technical standards.

[25] The Commission notes that in the cases where the IPCEI Microelectronics leads to the emergence of a standard essential patent, general antitrust rules apply in terms of licensing obligations on FRAND terms.

(157) The IPCEI Microelectronics will bring together several industrial players (e.g. equipment manufacturers as well as CAD tool manufacturers), whose products will be tools that can be used by all designers or manufacturers of integrated circuits. These players will retain all the exploitation rights in their commercial sector and will thus be able to make advances accessible to microelectronics players.

2.5.6. Dissemination via major European clusters in microelectronics

(158) The Member States point out that IPCEI Microelectronics will bring together directly 16 European partners and indirectly 370 partners[26] that are members in one of the major European clusters:

- 5 direct partners and 350 indirect IPCEI partners are members of the Crolles-Grenoble (Minalogic, France) cluster;
- 9 direct partners and 320 indirect IPCEI partners are members of the Dresden (Silicon Saxony, Germany) cluster;
- at least 2 indirect IPCEI partners are members of the Leuven-Eindhoven (Belgium and the Netherlands) cluster.
- Additional direct and indirect partners recruited as part of the IPCEI Microelectronics to strengthen the first ever Compound Semiconductor Cluster, centered around South Wales (UK), in the technology field of compound materials
- Additional direct and indirect partners recruited as part of the IPCEI Microelectronics to strengthen the European microelectronics clusters, centered on the ecosystems mainly located in Italy[27], in the technology fields of energy efficient chips, power semiconductors and sensors.

(159) These major European clusters cover more extensive areas than those of the IPCEI Microelectronics; they are also expected to continue, and to extend their coverage with the arrival of new partners.

(160) The Member States point out that clusters contribute to the dissemination of knowledge and know-how. Many partners belonging to the mentioned European clusters are involved directly or indirectly in IPCEI Microelectronics and will promote the dissemination of knowledge and know-how developed in IPCEI Microelectronics, notably through the following:

- R&D on joint programs - teams of direct and indirect IPCEI partners who are members of the clusters are integrated into the cluster research teams;
- Knowledge sharing and feedback - partners in the three clusters and those of the IPCEI will be able to share their own knowledge and experience. IPCEI Microelectronics will lay the foundations for numerous and intensive exchanges between the actors of the different European clusters;
- Production of joint publications and dissemination of knowledge to the different clusters involved.

[26] “Indirect partners” are considered by the notifying Member States the companies which are not IPCEI partners (incl. aid beneficiaries and ROs), but are cooperating in some way with the IPCEI partners.

[27] Around Agrate Brianza (in the North), and Catania (in the South).

(161) The results and innovations resulting from the work of the IPCEI partners who are members of these clusters will indeed be directed towards other industries in the sector, which are also members of the clusters. There will also be a dissemination of knowledge, via cluster members to their own partners and ecosystem. As a result, several ecosystems will benefit from the results of the IPCEI Microelectronics. Essentially, the benefits of knowledge dissemination will not be captured by direct partners in the IPCEI Microelectronics. As a result, key players in these clusters will be able to benefit from the knowledge and know-how developed within the framework of the IPCEI Microelectronics.

2.5.7. Spillover effects in first industrial deployment

(162) The foundry partners within IPCEI Microelectronics will provide multi project wafer (MPW) access within the FID phase for external research and industrial partners. Initial qualification actions are mandatory before granting this access and will be followed-up until end of the safe launch of certain technologies. Based on this early access SMEs and other partners will be enabled to shorten their time-to-market.

(163) A second way to address spillover in FID, besides the MPW, is by opening the access to IPCEI Microelectronics consortia facilities which are flexible enough to host prototype in small series with dedicated processes (not simply accessing part of well-defined processes, something that big foundries or IDMs can hardly do). Due to the technology and know-how improvements allowed by IPCEI Microelectronics, also the "small" partners (SMEs and/or ROs) will offer an active support to fabless companies, or companies which are not directly involved in IPCEI Microelectronics.

(164) The Member States provide several examples of spillover during first industrial deployment:

- *[...]* FID phase in IPCEI Microelectronics will leverage subcontracting with industrial partners. These collaborations are extended to equipment manufacturers (*[...]*), raw material supplier (*[...]*) and metrology players like *[...]* present all over Europe.
- The technology developed in IPCEI Microelectronics by *[...]* will be opened to small volume markets in a model of agile foundry.
- *[...]* will offer Job-shop services in *[...]*. Furthermore a machine system for the *[...]* will be set-up in order to evaluate the *[...]* at customer sites. *[...]* will provide those offers within the first industrial deployment phase for external research and industrial partners too.

2.5.8. Spillover effects in downstream markets

(165) The Member States state that the project will lead to significant spillover effects in downstream markets. As a result of IPCEI Microelectronics, the partners will enter into supply and cooperation agreements with third parties outside IPCEI Microelectronics. Such third parties are in many cases located outside the notifying Member States.

(166) The customers and cooperation partners of the IPCEI partners will benefit in many ways from the project. IPCEI Microelectronics will enable them to develop new product applications and designs and to acquire specific skills as

well as know-how, which again can be used in cooperation with third (non-IPCEI-) parties. As a consequence, this process will lead to positive effects on the downstream level which extend to a wide part of the EU.

(167) As an example *[...]* will enable new collaboration links in downstream markets by offering integration technologies for complete new system integration aspects. These capabilities can be used by automotive or industrial partners to collaborate with other semiconductor manufactures for unique system solutions by combining the expertise and capabilities of the partners.

(168) *[...]* will use *[...]* programmes *[...]* as an enabler to settle sustainable partnerships with key end-users all over *[...]* and align on the final demand roadmaps. *[...]*.

(169) Components developed by *[...]* will be enablers for other markets such as medical implantable application. ECSEL or PENTA programmes will be used to open new collaborations down the value chain and extend the usage of these components.

2.6. Progress beyond the state-of-the–art of the R&D&I and FID activities included in the IPCEI Microelectronics

(170) The Member States submit that IPCEI Microelectronics activities in the technological fields concerned will seek to overcome the below mentioned technological risks and will bring the following progress beyond the state of the art in the respective fields:

2.6.1. In TF1(Energy efficient chips)

(171) The Member States explain that Moore's law of scaling transistors down in size, and thereby enhancing performance while at the same time reducing energy consumption, chip dimensions (mm^2) and costs of single functions, has hit a wall with bulk technologies around the 28 nm feature size. The envisaged FDSOI technology enables the down-scaling to structure sizes of 22 nm. Scaling is not an end itself, but in the case of FDSOI it allows to move beyond the limiting parameters of the so-called Bulk-CMOS while providing a cost- and energy-efficient alternative to so-called FinFET transistors. This allows TF1 to aim with FDSOI technology at reducing the static device leakage to only 1 pA/µm and even achieve further leakage optimization via back-biasing.

(172) As for the second envisaged CMOS RF-SOI technology, this low power technology rooted in Europe drives industrial roadmaps in the More-than-Moore technology domain adding connectivity features on existing logic, mixed-signal and RF System-on-Chip (SoC) components. The main challenge is to accomplish different RF-SOI *[...]* platforms to cover the frequency range from 0.7 GHz to more than 100 GHz and answer the superior radio performance, increased number of bands and bandwidth with an increased level of integration requirements related to 5G *[...]*.

(173) *[...]*.

(174) These TF1 challenges concern the different phases of a component maturity from R&D&I to FID phase. Classical R&D&I work refers to a scientific way of

experimenting (via Design of Experiments, DoE) with the needed amount of statistical precision and subsequent analysis of the data. These activities mainly cover the development of technologies. It includes all the work on materials, transistor structure, design environment, process, performance, cost, and variability trade-offs. At the end of this phase a new technology is defined and ready to move in the FID phase.

(175) The Member States further point out that during the FID phase, there is still a lot of R&D&I activity related to the manufacturing aspects of the technology. This includes the improvement of process reliability and repeatability in order to reach a truly mature process level. R&D&I in FID refers to the same way of working like in "classical" R&D&I but with even larger statistical base and smaller process variation closer to the envisaged final process. Due to this, tiny effects can be detected and inter- or counteraction of multiple effects are explored, which leads to superior process control and stability.

2.6.1.1. The power challenge and the FDSOI opportunity

(176) TF1 is one step to realize the full potential of the FDSOI technology, invented and further advanced in Europe. The benefits of FDSOI in comparison to the predominant FinFET (Fin Field Effect Transistor) technologies (named after the fin-like shape of its three-dimensional transistors) can be succinctly summarized as follows:

- FDSOI steps up integration densities to the next node-generation, capitalizing on existing infrastructure and manufacturing investments;
- Power dissipations of next technology nodes is going up, but FDSOI offers a significantly lower power footprint than comparable technologies;
- Process complexity is generally exploding due to stringent process complexity increases. In this context, FDSOI offers simplicity in processing;
- FDSOI capitalizes on the strengths of the European supply infrastructure from wafer sourcing up to IP-offering and Services (http://things2do.space.com.ro/)

(177) Scaling technology below 28nm results in increased production steps and cost. FDSOI, esp. at the 22nm node, will offer excellent performance in an energy-efficient manner and, due to estimated decreased manufacturing process complexity, at advantageous cost. That combination provides a real opportunity to continue European technology advances for key markets like Automotive, IoT, and 5G.

(178) There is a wide range of new applications like embedded computing applications where power budget is typically very limited and must be balanced with performance targets. A good example for this are advanced driver-assistance systems (ADAS) applications, where designers must constantly find compromises between required performance and a very limited power budget (*[...]*). With its ability to run on very low supply voltages, FDSOI is attracting interest as the reference technology for all embedded computing applications.

(179) The Member States provide the following summary of where the partners in TF1 will go beyond state of the art:

- Development and first industrial deployment of advanced substrates compatible with FDSOI requirements at the 28nm, 22nm and eventually 12nm node. *[...]*.
- Development of new design methods and environment for 22FDX in order to extend the 22-FDX technology applications to make maximum use of all possible digital or analogue operational functions. *[...]*.
- Development and first industrial deployment of specialized version of the FDSOI technology to fit new user requirements in Automotive and IoT. *[...]*.
- *[...]*.
- Development of a versatile System on Chip (SOC) platform as the basis for product design for a very broad range of IoT and Industry 4.0 applications in 22FDX.
- Development of a new challenging FPGA (Field Programmable Gate Array) structure for programmable logic. *[...]*.

2.6.1.2. The wireless communications and radio frequency technologies

(180) The Member States submit that the current trend in wireless communication is toward more bandwidth, less latency, more mobility with reduced power consumption. All of these challenging requirements are strong drivers of innovation at the technology level. At the same time, substantial efforts are essential at materials, substrates, design and architecture levels to reach the ambitious goals of this IPCEI Microelectronics.

(181) The boom of connected objects for automotive, healthcare, logistics, security, as well as general daily life will require high performance, low cost, energy efficient electronics components for Radio Frequency (RF) communication. Next generation 5G communication technologies bring a new opportunity for Europe to develop in a sustainable manner an RF ecosystem addressing cost and performance needs for Front-end Modules and bringing new 5G connectivity standards potentially into new GHz ranges.

(182) As a baseline:

- RF-SOI technology has demonstrated switch performance and integration capability, and therefore became a 4G compatible standard *[...]*.
- FDSOI has shown unique RF/analogue performances *[...]*.

(183) The Member States point out that the following progress beyond the state of the art is required at technology level:

- Development of a new RF-SOI advanced wafer substrates roadmap moving from 200mm to 300mm wafer in response to 5G requirements *[...]*.
- Development of RF components (*[...]*) with higher figure of merit in response to the need of bandwidth expansion *[...]* for the forthcoming 5G standards. *[...]*.
- *[...]*.
- *[...]*.
- Creation of IP supporting new wireless communication standards for Automotive, IoT and other applications benefiting from new FDSOI technology performance in the gigahertz spectrum. All participants are

committed to develop Intellectual Property (IP) such as patents and trade secrets. *[...]*. The IP will be a mix of public and confidential IP with the intent within in TF1 to be as open as possible in order to facilitate the best possible uptake of technology deriving from TF1. Standardization activities are not foreseen in TF1.

- Integration of RF capabilities *[...]* for applications in space.

2.6.1.3. Energy efficient storage and embedded Non Volatile Memories challenges

(184) Embedded Non Volatile Memory (eNVM) is a type of memory that can retrieve stored information after having been power cycled (power turned off, power turned on). eNVM allows to finely integrate CMOS technologies with permanent memories, which keep their data when the chip is not constantly powered. Those types of devices are needed for security applications such as banking cards but also safety-related applications such as automotive electronics. The overall challenges are thus to increase the density of the embedded memory, along with the logic element, while maintaining a high level of robustness and low energy consumption to satisfy the needs of future systems, including improved connectivity.

(185) The main progress beyond the state of the art will be in the domains as detailed:

- Embedded non-volatile storage with new, disruptive technologies *[...]*.
- *[...]*.
- Expand the capabilities of E^2PROM (Electrically Erasable Programmable Read Only Memory) technologies *[...]*.
- Introduction of a new PCRAM (Phase Change Random Access Memory) technology at the 28nm FDSOI node for microcontroller products (*[...]*).
- New design platforms using FDSOI and eNVM, in order to improve the power efficiency *[...]*.
- Introduction of new eNVM technologies such as OxRAM (HfO2-based oxide-based resistive memory), *[...]*.

2.6.2. In TF2 (Power semiconductors)

(186) The Member states explain that the evolution of power semiconductors has arrived at a level where packaging restricts the achievable performance of the final device. This statement holds for established silicon as well as new SiC and GaN technology with their ultra-fast switching and high power density. A specific feature of power semiconductor technology is that the entire supply chain is integral to innovation. The whole process – from design until manufacturing – is important for the performance and the quality.

- New power Technologies include alternative materials like GaN or SiC *[...]*;
- New High Voltage (HV) technologies for power Integrated Circuits (ICs) and integrated smart power solutions driving to better energy saving and efficiency improvement for Automotive and Industrial applications;
- New Assembly Techniques include new packages with increased functionality, cost effectiveness and better flexibility as well as a co-optimization between the chips and their package;
- FID according to Industry 4.0 technology to optimize the trade-off between flexibility and efficiency;

- Improved and assured quality and reliability during the implementation of new technologies and FID is an indispensable requirement.

(187) The Member States further provide the following summary of the R&D content of the R&D&I projects and FID activities within TF2:

(a) R&D&I projects:

- *[...]*
- New dicing technology which can be used for all types of wafers:
  - *[...]*,
  - *[...]*
- Development of innovative dielectrics, new electrodes and associated process steps for advanced capacitors
- *[...]*
- Development of RF (Radio Frequency) GaN frontend-technology for power applications
- *[...]*
- *[...]*
- *[...]*
- Power technologies (*[...]*) for new power devices in emerging applications
- New process technologies for System in Package mastering the big challenges in the packaging area
- *[...]*.

(b) R&D in FID activities:

- *[...]*
- Migration of new smart power and power discrete technologies based on GaN/Si to larger technology platforms (200 mm)
- *[...]*
- Development of appropriate GaN die preparation and test developments
- First process parameters optimization
- Development of FID test solution for integrated power packages
- Characterisation and modelling for robust and reliable power technologies incl. tests during FID
- Yield analysis and improvement for complex integrated smart power technologies
- Implementation of advanced process monitoring as well as advanced process control methodologies

(c) By the combination of R&D&I projects and R&D in FID the following is aimed to be achieved:

- Development of integrated power solutions for motor control and functional safe DC/DC applications *[...]*
- Development of corresponding strategies and solutions for failure analysis, reliability and test
- *[...]*
- *[...]*
- Development of BCD technologies working at high voltage and *[...]*
- Development of new advanced passive technology to be used in several applications *[...]*.
- *[...]*.

- Smart power in mixed signal technologies and high power discrete technologies with an emphasis on automotive applications
- Power GaN device developments and FID for power application
- Advanced Silicon device developments and FID for power and IoT applications
- *[...]*
- *[...]*
- Development and implementation of real-time fab intelligence processes and other innovative fab logistic solutions for existing and new semiconductor processes and equipment to enable highly flexible manufacturing of small and medium production volumes up to FID of these techniques

2.6.2.1. Complementary Co-operation

(188) The various technological challenges are also tackled within precompetitive European R&D&I programmes like PENTA or ECSEL. Both, large European projects under ECSEL as well as smaller projects like the H2020 research and innovation programmes, are a platform for the exchange of innovative ideas and see the collaboration of IPCEI Microelectronics members and other EU companies in the development of new technologies. The partners of TF2 cooperate with the other TFs and within TF2 preferably on the base of the ECSEL Multiannual Strategic Roadmap (MASRIA), in order to achieve a coordinated workflow.

(189) Beyond this, in the Member States' view, there is collaboration to improve standards that support the EU willingness to create a safer and green ecosystem. On this level, research and innovation create the precondition for a sustainable, knowledge-based ecosystem for power semiconductors and semiconductor industry in general.

2.6.2.2. Materials and Technologies

(190) The Member States note that today, the majority of power applications are based on Silicon (Si). Especially for Si based power devices, but not only, FID according to Industry 4.0 is key to enable best cost-performance-ratio for future market applications. Related activities include:

- meet improved uniformity requirements within the structures (within chip, across wafer, wafer to wafer) leading to higher functional yield and increased reliability;
- reduction of defect density for the devices of tomorrow from a single component to the full assembled equipment for all wet chemistry related processes.

(191) Driven by efficiency requirements for some applications and power density needs for others, semiconductor performances and the thermal management on their packages have become the centre of the focus in the power electronics industry.

(192) SiC and GaN are being integrated in new generation power converters beyond state-of-the-art. Power semiconductor devices based on compound semiconductors and especially wide bandgap materials with a bandgap > 3 eV (Si 1.12 eV, SiC 3.0 – 3.23 eV, GaN 3.37 eV) offer new possibilities:

- SiC provides:
  - *[...]*
  - *[...]*
  - *[...]*
- GaN enables:
  - *[...]*
  - *[...]*
  - *[...]*

(193) Benefits for the applications are:

- Switching at higher frequencies than conventional silicon can improve power density by shrinking the size of passive components. It can also help to save energy on cooling the overall system. Low charge and dynamic performance in reverse conduction compared to silicon alternatives can enable more efficient operation in today´s applications at existing frequencies.
- The much higher breakdown field strength and thermal conductivity of SiC devices for example allows semiconductor suppliers to create devices that outperform silicon alternatives across a range of temperatures – *[...]*.
- Main applications for GaN products are power supplies optimized for the highest possible efficiency for use with high-performance servers in data centers. *[...]*, power supplies using GaN can be designed differently from silicon-based power supplies. Depending on the configuration, this can help realize system cost advantages. The higher efficiency reduces cooling effort and cuts the cost of heat sinks and air conditioning. *[...]*.
- At the same time the compactness, i.e. the power density, measured in Watts per cubic centimeter, can be increased. Power density is important because every square meter of floor space in these air-conditioned spaces is very expensive. The development of the next generation of GaN technology makes it possible to realize smaller and thus more cost-effective transistors. This will support the introduction of GaN technology also in price-sensitive markets such as motor control units in washing machines and air conditioners.

(194) With higher power densities and high reliability requirements, the package materials and structure become a key aspect for innovation, *[...]*.

(195) These advanced technologies will enable a significant efficiency increase in generation and distribution of electric power covering the range from gigawatt (GW) power (e.g. in energy transmission lines) down to the very low milliwatt (mW) power needed to operate a mobile phone. Mobile applications such as electric vehicles will benefit from smaller and lighter weight power packages enabled by ultra-fast switching. Reduced costs of production and materials allows for an increasing share of renewable energy while maintaining availability of electricity with highly reliable power electronics.

2.6.2.3. Results to be achieved

(196) The Member states explain that new power technologies in combination with new assembly techniques will also lead to more robust and durable products required for applications in harsh environments such as industrial welding. New

smart power technologies will further increase the reliability and functional safety of uninterruptible power supplies (UPS) which are, e.g., the backbone of the IT systems of banks and insurance companies.

(197) Concrete technical progress and product improvements for power devices to be achieved within TF2 include:

- improvement of heat dissipation, *[...]*;
- application of new thermal concepts, *[...]*;
- improved power density and reduced form factors *[...]*;
- *[...]*;
- introduction of Industry 4.0 capabilities will lead to more stable processes and thus improve reliability and robustness, major differentiating factors for European electronic component and device makers;
- robust devices have a higher durability which reduces the electronic waste

(198) Industry 4.0 capabilities should enable an increased flexibility of the processes for smart power devices supporting different applications.

2.6.3. In TF3 (Sensors)

(199) The Member States explain that in very generic terms, the success for smart sensors relies on advances in the "PPPV" space (Power, Performance, Price, and Volume). To those parameters one has to add at least reliability and security (RS). Indeed, the sensors are the first element in the chain of safety or security critical systems, in respect of driving assistance, communication network control, authentication, health applications etc. Their failure to deliver accurate information induces a system failure. Thus, the development and FID efforts in the TF3 of IPCEI Microelectronics will aim at improving the positioning of smart sensors in this six-dimensional space: PPPVRS. Those improvements can be continuously used to create new and extended system functionalities or even enter new product markets.

(200) It is difficult to predict "quantum leaps" but such events occurred in the recent years, and have been driven by some of the participants of TF3. For instance, the capability to miniaturize and reduce the power consumption of accelerometers, gyroscopes, magnetometers and pressure sensors (sensors controlling movement and position) by several orders of magnitude over a few years, allowed to create light-weight drones, which was impossible before. *[...]*.

(201) Among the specific challenges and progress that are expected and needed to ensure the pervasion of sensors are measurement-performance improvement, new parameters to be measured, security and safety associated to sensors, integration challenges, reliability and quality of measurement, new materials and methods to support the previous progresses.

(202) The measurement performances will be improved in terms of sensitivity of all parameters (signal-over-noise ratio at a given measurement frequency and energy per measurement), number of simultaneous measurements (e.g. number of pixels in an optical sensor of a given type). *[...]*.

(203) New parameters are being measured by highly integrated smart sensors. In recent years, highly sensitive accelerometers, gyroscopes, visible image sensors have become mainstream. Magnetic sensors, pressure sensors, microphones,

infrared in various spectral ranges image sensors, ranging sensors, spatial and ranging sensors, highly integrated chemical sensors should be brought to a level of FID. On top of extending the parameters list, some sensors include also the actuation capability, which integrates a large part of the feedback chain (sense and react), e.g. by using piezo-electric materials in MEMS. For optical sensors actuation also includes illumination when needed and or active focusing. *[...]*.

(204) Security and safety associated to sensors is a very important challenge that needs to be tackled at all the levels of the system from the sensing device through the whole digital chain. Considering security at sensors' level, several aspects will be addressed. Confidence in the sensor ability to sense with the specified accuracy in the intended application, will be addressed by developing and integrating self-test procedures which will be on case by case basis and often require important development. Confidence in the integrity of the data generated by the sensor will be addressed by introducing strategies (in software and hardware) to ensure unambiguous data source identification and to prevent sensor hacking. *[...]*.

(205) Integration and packaging is one key for smart sensors since sensors are inherently in contact with the physical world and are often made of highly heterogeneous parts, e.g. parts made of different materials, in close interaction. Among the challenges are tight integration in a System-in-Package approach, *[...]*. *[...]* In TF3 this µTP integration technology will be further developed towards the FID phase and should be the 1st ever industrial offering for heterogeneous integration like III-V materials from TF5 into smart sensor systems or special components from TF1 to smart sensor platforms.

(206) Reliability and quality will have to be improved to enter various application domains and are paramount in view of high volume needs for sensitive applications such as automotive. They require precise models and characterization inducing large efforts during the R&D&I and the FID phases. *[...]*.

(207) Numerous new materials for mechanical drives, optical surfaces and gas-sensitive layers (non-exhaustive list) will be developed or brought to an industrial maturity and extensively modelled in IPCEI Microelectronics in order to be used.

(208) Manufacturing concepts and methods for novel devices should combine standard basic process steps with dedicated innovative processing to achieve a cost-optimized solution that fulfill the requirements of the European market. *[...]*.

(209) When it comes to implementation, the R&D&I during FID is considered more application, device and system specific concerning particular requirements. It is not limited to isolated process modules. Only on the device level all interacting effects of a manufacturing strategy are captured and become visible via device and system specific parameters. The manufactured result is subject of the evaluation during FID. The resulting R&D&I is required feedback based on FAILs derived from the applied qualification scenario. Such R&D&I activity is highly undesired, but from experience, it needs to be planned and considered. Consequently, the FID related R&D&I is very likely to go well beyond the classical R&D&I approach, as it needs to handle the unwanted, unplanned and

most likely the unknown. Qualification Fails are not planned, but they will occur. Typically the search for and even the right approach to examine the underlying FAIL mechanisms is a venture on itself. The evaluations of appropriate analysis tools are subject of research. In response to the findings, a redesign on the system level can be considered as a very comfortable scenario, although it is already related to R&D&I effort, which might exceed very quickly a normal level of re-engineering (simulation, etc.). But often the feedback loop turns much deeper and already qualified and released base technology modules (process recipes, design rules, etc.) need to be re-considered and significantly changed.

(210) The Member States further provide the following summary of the R&D content of the R&D&I projects and FID activities within TF3:

(a) R&D&I projects:

- Develop innovative implantable MEMS-based sensor arrays and systems to enable electrical interaction with neural tissue for novel biomedical applications
- Enabling technologies and design for innovative CIS and TOF devices, *[...]*
- 3D Integration (*[...]*) process for high sensitivity image sensors *[...]*
- Sensor technology for radar applications (*[...]*)
- Sensor technology for automotive applications *[...]*
- Sensor technology for mobile communication and Internet of Things
- *[...]*
- High-performant motion sensor for CE (consumer electronics) applications
- Innovative CIS, involving successive generations of pixel, progress on integrated optics and Filters
- Innovative vertical magnetic sensors
- Time-of-Flight based innovative products, *[...]*
- Enabling Technologies involving various bonding and multilayer approaches, *[...]*
- Innovative Integrated Vision Systems, involving inclusion of dedicated IPs
- Innovative Ultrasonic Sensor Systems for Automotive Applications
- MEMS micro-actuators and intelligent devices technologies *[...]*
- AMR Magnetometer for E-compass applications *[...]*
- Thermal-based perception systems to Mobility (mainly Automotive) and Society applications
- Development of an innovative open-access analog mixed-signal technology platform suitable for the manufacturing of sensor IC's targeting multiple areas like automotive, industry, medical, IoT and integration of various functionalities (like embedded automotive qualified non-volatile memory, special sensing capabilities...)
- Set up sensor labs for R&D as well as sample and product verification

(b) R&D in FID activities:

- Setting-up clean room facility with dedicated and customized micro-machining equipment and complementary laboratories for R&D

- R&D for functional testing, reliability and quality as well as assembly and packaging
- Sensor developments for functional testing, reliability and quality as well as assembly and packaging
- Flexible process technologies for pressure and magnetic sensors
- Systemic effects on the value chain – upstream for equipment and service suppliers and downstream for system designer for consumer, automotive, energy. (RB)
- Unique semiconductor "FID infrastructure and "FID-equipment" will be developed and implemented *[...]*, setting new standards for automation
- *[...]*
- Technology and product robustness analysis, modelling, and improvement for MEMS, magnetic, and smart optical sensors
- Functional testing, reliability and quality as well as assembly and packaging of MEMS, magnetic, and smart optical sensors
- FID for the next-generation magnetic-field sensors with new standards with regards to performance and quality.
- FID for new thermal systems, compliant especially with the automotive applications.
- Standardize fully qualified open-access process blocks for new wafer-level bonding technologies and special piezo-electric material integration to serve different applications and to reduce time-to-market for end users
- Develop heterogeneous integration *[...]*
- All additional design of experiment needed to bring the developed processes at level of robustness compatible with automotive and other application standards.
- Process tuning and stabilization, characterization and improvements of the first component realization with technologies developed during R&D&I phase - *[...]*.

2.6.4. In TF4 (Advanced optical equipment)

(211) The innovations, which are planned in TF4 are manifold. A new, technically highly innovative disruptive imaging technique will be developed up to FID for EUV scanners: *[...]*. It enables a numerical aperture (NA) previously unattained for EUV optics (Hyper NA). The technique requires a totally new optical concept. Instead of using a group of about 30 single quartz glass lenses as imaging system, an ensemble of about 10 reflective mirrors will be developed to use them for imaging the features of a EUV photomask onto the semiconductor wafer. This fundamental change of the optical concept is required because of the extremely strong absorption of the EUV light in quartz glass and in gaseous matter, which does not happen for Deep Ultra Violet (DUV) light. Therefore the whole optical system has to be housed in a huge high vacuum tube. Also a new mask substrate has to be developed for EUV because the mask can be used in reflection only, and not in transmission as it is state-of-the-art for masks.

(212) The light for imaging the mask features, which comprehend the chip design, is as already mentioned EUV, i.e. 13.5nm. This wavelength is about 15 times smaller than the smallest DUV light wavelength, i.e. a wavelength of 193nm, which is currently used in all advanced chip manufacturing fabs. Using EUV light will give an extraordinary resolution improvement potential that has never

been seen in such an extent in the history of electronics chips manufacturing before.

(213) A complete mask projection system needs also an illumination system for illuminating the EUV mask with EUV light. Therefore the Hyper NA EUV projection system need to be complemented with an appropriately designed EUV illumination system, which has to adapt perfectly to the requirements of advanced chip designs. The individual optical elements of the EUV illumination system consist only of mirrors instead of quartz lenses as for DUV illumination systems. In fact, the EUV illumination system will consist of several thousands of mirrors of millimeter size, many of them individually angular controllable mirrors of millimeter size. Compared to the state-of-the-art DUV illumination systems, this EUV illumination system will also require a highly disruptive optics manufacturing technique.

(214) The Member States point out the major technical challenges for realizing a mirror based projection objective result for the projection objective from the following specifications:

- Surface areas of mirrors up to $1m^2$, i.e. about 10 times larger area than lenses of the DUV objective.
- Mirror surface manufacturing precision smaller than 50pm, i.e. less of the half of a Si atom diameter. This precision has to be reached also across the largest mirror surface (see (i)).
- Extreme mirror surface shapes. This requires the development of new disruptive mechanical material abrasive techniques to achieve the precision and material removal efficiency. The mirror grinding efficiency has to be improved by a factor of 1,000 (DUV lenses have always rotation-symmetric surface shapes).
- Extremely large deviations from a spherical surface, which requires an extremely precise control of the mechanical abrasion technology.
- Highly precise material removal techniques based on ion beam mirror surface polishing. The technique must be able to locally remove tiny clusters of a few atoms.
- Single digit picometer precision (< 10pm) for the mirror surface metrology. This is multiple times more than the state-of-the-art metrology precision.
- Sub-nm precision for the mirror integration to a projection objective. That means, along the several meters long optical axis of the EUV projection system the imaging mirrors have to be placed with extremely high longitudinal and angular precision and kept on place.

(215) EUV projection objectives will be also significantly different in size and weight compared to the DUV lens. The EUV objective weight will be about 12 tons, i.e. more than 10 times of that of the heaviest DUV objectives. About the same relationship results for the volumes of the objectives. All-in-all the described technical specifications for the EUV objectives are by far absolutely unmatched, i.e. remaining a huge technical challenge to develop all techniques needed to realize first samples.

(216) Technical challenges for the illumination system development and FID are:

- Defining appropriate technical means for the in-coupling of the light into the optical channel, i.e. coordinating several thousands of small mirrors,

most of them having the capability of continuous two-dimensional angular switching.

- Realizing suitable mechatronics solutions for efficient and precise light beam deflection to achieve optimum illumination of the EUV mask and mask imaging quality.
- Fabrication of thousands of highly integrated reflective switching elements of millimeter size.
- Manufacturing of small facet shaped mirrors with reflective layers, which cope with extremely high EUV irradiation densities.
- Managing the strong thermal load of the optical components caused by absorption of the EUV irradiation (up to 500W), i.e. handling the optics components cooling appropriately.

(217) The Member States also point out that for the development and integration of the Hyper NA EUV optics about 60 optics manufacturing tools and instruments need to be developed and tested. Most of these tools and instruments are not commercially available, since they need to meet very specific technical requirements and specifications. They have to be developed and manufactured with very specific performance. Illustrative examples for such equipment are tools for mechanical mirror surface processing like grinding, lapping, polishing, EUV multi-layer deposition systems, electron-beam irradiation systems, ion beam irradiation tools, various metrology tools such as for EUV reflectivity, surface roughness, contamination, and metrology tools for projection objective mirror figure and illumination mirror facets shapes measurement, vacuum cleaning systems for optics components and modules and many tools more. This requires strong development efforts, very close technical collaboration with the manufacturers of such equipment or – in case of in-house manufacturing – very specific technical advancements.

(218) The Member states affirm that a key development goal within the TF4 is to source the EUV resolution potential for future chip miniaturization. On a large scale this pattern shrink resource can only be accessed, when defect free EUV masks will be timely available at the EUV technology manufacturing entrance point. These EUV masks are indispensable for the EUV lithography introduction in chip manufacturing.

(219) Therefore an important goal will be to develop EUV masks and by this contribute to enabling future manufacturing of highly integrated devices.

(220) For future technology nodes, lithography solutions will significantly increase the challenges on the mask maker. Key indicators for these challenges are a strong pattern shrink by up to a factor of 5 compared to DUV masks, the all-reflective performance of the mask, new mask substrate materials, new EUV reflective material stacks, new absorber etching techniques, totally new mask defect and inspection scenarios and many more.

(221) For future technology nodes, lithography solutions will increase the challenges on the mask manufacturing technology dramatically. Key indicators for these challenges are - besides a strong pattern shrink - a corresponding all-over placement accuracy and line-width uniformity improvement of the mask features compared to transmittive DUV masks. The all-reflective performance of the mask as a new challenging element has to be controlled. Complex

material stacks with up to 44 layers compared to 3 layers on a DUV mask have to be processed with completely new processing techniques. The development of new, disruptive patterning and etching techniques is required. In addition, new mask defect mitigation, repair and inspection scenarios being much more complex than for state-of-the-art DUV masks have to be developed and implemented to enable defect free EUV masks.

(222) Furthermore, an optimization of reticle patterns coupled with source mask optimizations will be needed to achieve the lithographer's patterning goals. The reticle pattern optimization portions entail the use of complex rule-based optical proximity correction. This results in features on the mask posing huge challenges to the mask manufacturing process such as the continued shrink of sub-resolution assist features (SRAF) sizes down to 20 nm, curvilinear SRAF shapes and other highly complex mask geometries. Considerable capability improvements compared to state-of-the-art mask making methods are necessary to meet the new tight requirements particular according pattern fidelity, feature uniformity and placement accuracy in the nm regime. In addition, to meet these challenges, new materials have to be introduced and a new generation of electron beam writers is required deploying several hundred thousands of electron beams on a low sensitive resist. The introduction of such a system calls for a complete new technology and requires fundamental evaluation and development of the lithographic process.

(223) Main challenge of EUV masks is to manufacture defect free masks. Driven by the complex mask stack of absorber on a multilayer mirror and the reflective nature of the mask, new defect types and mechanism compared to state-of-the-art transmission masks appear. Therefore, new innovative processes have to be developed to mitigate defects covering the whole mask manufacturing flow, i.e. identifying defects on blanks and mask-level, repair of different defect types, final validation of repaired features, and cleaning of the mask with the needed quality, effectiveness and repeatability. In addition, to ensure the defect free status of a mask at point of use, the introduction of a pellicle is mandatory to shield the mask surface from falling particles during transport and use of mask. Due to the nature of the pellicle and the special fixation using a removable frame on the mask, a completely new tool set is needed. The requirements are not comparable to existing processes and demand the implementation of a completely new infrastructure with new tools and advanced specifications compared to state-of-the-art optical masks.

(224) A line for advanced EUV masks will be setup, which requires R&D&I activities for the development of a manufacturing flow of much higher complexity then for state-of-the-art photomasks. A variety of specific tailored manufacturing tools and instruments will need to be acquired. This includes the definition of tool and instruments specifications, common development activities with the suppliers, the installation of the tools and instruments, their integration in the mask manufacturing line, the process setup and technology release. Then the technology development for the various unit processes as described above will be done and combined to a complete mask manufacturing process. The introduction of this innovative imaging technique will have deep impact on the mask manufacturing process, and will require and set new standards for chip design, data conversion, pattern writing, mask inspection, mask repair and process control.

(225) As regards the R&D contents in the FID activities, the Member States submit that the FID related R&D activities for the EUV optics start after the optics system's integration into the EUV scanner. This R&D&I will be triggered through feedback on the optics performance by the IC manufacturers integrating the Hyper NA EUV exposure tool in their lines for evaluation and technology development. Obtained technical response will induce further R&D&I at Zeiss. In addition, the optics manufacturing process will be further improved. Typically, the specifications of the optics system will be tightened after the first prototypes have been made available. That means, optics components, optics modules and the whole optics system will have to be made with increased precision and higher yield. This induces substantial R&D&I efforts.

(226) A comparable application and improvement process will be pursued for EUV mask making. R&D&I activities in the FID phase are mainly focused on the identification of defect mechanisms and the development of mitigation strategies to achieve EUV masks with zero defects. For unit process stability improvement development, activities have to be executed to reach the all-over yield and cycle time target for a high volume mask line. In addition feedback will be received from scientific and industrial application partners, who will use the first masks. This will also induce FID related R&D&I for mask process performance improvement. It is expected that the mask specifications will be tightened in this time frame.

(227) Finally, Advanced Methods for Chip Manufacturing Enhancement will be developed focusing on solutions for logic electronic components. Until now this innovative technique has not yet been applied to logic devices. The focus will be on improving the printed feature size uniformity within the chip and within image field based on optimising the mask transmission using an advanced laser treatment. First learning will be performed for the DUV technology. In a succeeding step the technique will be used to improve the intra-field overlay. For the EUV technology this process is totally new. Key challenges will be defining the features out of a tremendous number of design features, which represent best the most functional- critical patterns of the chip layout. They need to be distributed well across the chip area and image field. The printed patterns have to be precisely measured in their lateral width and compared to their target values. The process of determining the positions of the features to be measured for the measurement tool (within the chip, image area, across wafer) needs to be organized in such a way that after their selection the measurement recipe for the metrology tool is generated automatically. For both, determining the positions of the features of interest in the chip layout as well as determining the measurement positions across the scanner imaging field in the electron beam metrology tool (SEM), an appropriate software has to be developed. Based on the measurement data the required transmission change on the mask substrate for applying the line-width correction need to be determined considering also feature displacement effects caused by process induced mask expansion. Both effects need to be balanced appropriately. Alternatively, if the focus of the AMCME application will be the overlay improvement within the chip, the process optimisation has to be inverse.

(228) For EUV masks such processes have also not been investigated yet. For the line-width control for EUV - instead of changing the mask substrate transmission – the substrate reflection needs to be adapted appropriately.

2.6.5. *In TF5 (Compound materials)*

(229) Future commercialisation of these technologies will require an innovative high volume pan-European source (~1 Million 150mm wafer-equivalents p.a.) of complex CS materials at an appropriate cost and scale point, complemented by an open-access CS Device Foundry, in order to provide Europe's major industries with on-shore supply of the critical components of current and future systems. Currently, CS materials are limited to 150mm epitaxial wafer (epiwafer) sizes and are relatively expensive. New applications and widespread market adoption will come from increasing the epiwafer size and lowering cost, by several key innovations, including:

- Further development of key CS technologies with IPCEI partners and external cooperation for new applications.
- Increased CS wafer sizes e.g. 200mm wafers and by combining CS with Silicon/Sapphire.
- Investment in large-scale first industrial deployment – open-access materials and device foundries.

(230) TF5 will deliver this vision by developing a unique CS Eco-system up to FID a unique CS Eco-system using, epi- and device-foundries, and Europe's leading supply (equipment/raw materials) and downstream companies (device fabrication, packaging, end-users), to focus on the most important end-to-end European CS device supply chains.

(231) The focus of the technological challenge will be to prepare, through FID, for future economies of scale, in bringing many new applications of CS materials to the fore. The main goal will be to ensure that CS wafers *[...]* are matured to first industrial deployment. *[...]*. The major challenge during the R&D&I in FID phase will be to work on scalability to larger epi-wafer diameters, enabling more efficient device fabrication, yield, throughput, reproducibility and economies of scale. This R&D&I in FID will provide for an FID phase, more suited to future manufacturing. *[...]*.

(232) Also, there will be major improvements through R&D&I in the device fabrication for ever-larger CS wafer sizes and to develop processes towards the efficiencies found largely in the LED industry to bring other optical CS device to beyond-state-of-the-art (B-SOTA) and to first industrial deployment. The challenges will be in FEOL and BEOL processing and in the packaging of novel applications of CS materials which will require substantial further R&D&I work during this FID phase. *[...]*.

(233) In addition to the development of the increased wafer sizes, through R&D&I during FID, new application areas for CS will be explored through the underlying R&D&I within the IPCEI Microelectronics project and through external cooperation with the many listed partners – and be brought to first industrial deployment. This FID phase at the industry partner will require additional underlying and substantial R&D&I work. *[...]*. This approach has great benefits for the open-access epi- and device-foundries and the IPCEI partners.

(234) The TF5 CS Ecosystem is best described by the "process flow" as depicted in Figure 3. Key strategic suppliers to the Epiwafer Foundry are from European

tool, metrology and chemical manufacturers. The 4 major materials supply-chains will support activities across micro-electronics and photonics; Power Electronics materials will support for example TF2; Photonics-based sensor materials will do likewise for TF3. CS Device fabrication, module and system FID will be performed by key strategic partners and an open-access device foundry from within TF5, providing capability for several strategic and key materials systems.

(235) The Epiwafer Foundry forms the primary materials developer and provider for the TF5 CS Ecosystem, supported by significant collaboration with other CS-Ecosystem partners, such as a novel open-access device foundry but with huge support form the Key Supply-Chain IPCEI Partners in developing supply chains and improvements through cooperative and collaborative feedback mechanisms. The concept allows for; enhancement of existing CS technologies; significant R&D for new devices; thereby allowing an evolution of Pilot activities towards FID.

(236) By proceeding with this highly innovative approach, the future production of high-performance epiwafers and devices to Europe's KET industries will be pushed beyond state-of-the-art. The innovative features and proposed multiple engagement "Open-Access" features of the Epiwafer and Device Foundries, will be positioned to provide epiwafer/device supplies from R&D&I towards FID.

(237) As a result of the above, major innovation will take place through a number of objectives within IPCEI Microelectronics collaborative projects. Several IPCEI partners will work jointly, together with cooperation partners (outside IPCEI) to target the development and first industrial deployment of 200mm-based photonics outputs based on integration and smart devices for novel applications with enhanced functionalities. This work will target data communications applications linked to enabling the next generation of data centres powering the internet, *[...]*. Innovation potential is employed for product and design in a foundry model creating an open-access resource for other photonics and CS-on-Silicon projects.

(238) A major initiative will be to extend a GaN-on-Silicon platform to 150mm, and thence elevate the wafer size towards first industrial deployment scale 200mm diameters. Power LEDs on 200mm wafers will present yield and photometric specification challenges, whilst monolithic μ-LED arrays for displays require a number of key developments and challenges (*[...]*) to enable new applications, in augmented/virtual reality (AR/VR). *[...]*.

(239) Another major development involving an IPCEI partner working collaboratively with cooperation partners, will provide for a future pipeline of high value-add components; multi-functional monolithically integrated PIN-TIA and APD-TIA for >100G datacomms applications; mm-wave/THz receivers *[...]*.

(240) In another major cross-partner collaboration within TF5, key innovation will be addressed through two key projects in infrared sensing and detection. Firstly, TV-format Infrared (IR) detectors capable of delivering the high performance levels required for astronomy applications (very low dark current and noise) will be developed. *[...]*.

(241) Further development and innovation will be sought in 2 major areas of Silicon Photonics and High-Performance and Cost-Effective BiCMOS Technologies. For Silicon Photonics this ranges from basic technology development to product introduction and market exploration, consisting of increasing data rate and decreasing form factor, *[...]*.

(242) Advanced optoelectronic devices and systems, e.g., smart and multifunctional LEDs, are also being addressed within TF5. Innovation will occur in several major subprojects within IPCEI Microelectronics. *[...]*.

(243) Finally, further development will occur through and customization of disruptive monolithically stacked photodiodes for application in opto-couplers, solid state relays, new sensors etc. Compared to state-of-the-art Si photodiodes these III-V components are smaller, provide more power output and have much better temperature stability. *[...]*.

2.7. Description of the aid measures

2.7.1. Selection of the participating partners in the IPCEI Microelectronics

(244) The notifying Member States inform about the following national procedures that have taken place for the selection of IPCEI Microelectronics participants:

- Germany published a call for projects on microelectronics in August 2016. 16 companies (including five SME) were selected.
- France has launched an open and transparent call for projects between December 2016 and February 2017. At the end of this call, seven companies and one RO replied and submitted project outlines.
- A consortium of companies approached the UK and Regional Governments in 2015. Initial interest was expressed by ten organizations. As a result of preliminary appraisal of the project proposals, four companies from the UK will participate in the IPCEI Microelectronics project.
- In Italy, current participants have been invited using the criteria of availability of a manufacturing site. A company (ST) and one RO (Fondazione Bruno Kessler) have agreed to join the formation of the IPCEI Microelectronics. A few more companies have been inquired but showed no interest.

(245) The Member States submit that assuming that entry rules can be defined by the Member States, from an industrial point of view there is the willingness to accept any new participation that fits into the IPCEI Microelectronics scope. The Member States consider the IPCEI Microelectronics as an open consortium and based on the Commission's decision, other entities fitting into the scope of the IPCEI Microelectronics may apply to their Member State authority at a later stage.

2.7.2. Total investment in the IPCEI Microelectronics

(246) The notifying Member States authorities indicated that the activities performed during the project qualify as "research and development" and "first industrial deployment" in the meaning of point 21 and 22 of the IPCEI Communication.

(247) They indicated that the total IPCEI Microelectronics project costs are estimated to be over EUR 7.8 billion, out of which EUR 5.3 billion for first industrial deployment and EUR 2.5 billion for research and development (see the table below).

Technology field	**First Industrial Deployment (FID)**				**Sum**
	DE*	FR	UK	IT	
Energy efficient chips	*[…]*	*[…]*			*[…]*
Power semiconductors	*[…]*	*[…]*		*[…]*	*[…]*
Sensors	*[…]*	*[…]*		*[…]*	*[…]*
Advanced optical equipment	*[…]*				*[…]*
Compound materials	*[…]*	*[…]*	*[…]*		*[…]*
Sum FID	*[…]*	*[…]*	*[…]*	*[…]*	**5,365**
Technology field	**R&D**				**Sum**
	DE*	FR	UK	IT	
Energy efficient chips	*[…]*	*[…]*		*[…]*	*[…]*
Power semiconductors	*[…]*	*[…]*		*[…]*	*[…]*
Sensors	*[…]*	*[…]*		*[…]*	*[…]*
Advanced optical equipment	*[…]*				*[…]*
Compound materials	*[…]*	*[…]*	*[…]*		*[…]*
Sum R&D	*[…]*	*[…]*	*[…]*	*[…]*	**2,529**
Sum total	***[2,580 - 3,367]***	***[1,633 - 2,130]***	***[317 - 413]***	***[1,950 - 2,543]***	**7,895**

**: in funding period (2017 – 2020)*

Table 2: Estimated total costs per technology field, per type of activity per Member State, in million EUR

2.7.3. Aid Beneficiaries and aid amounts

(248) The companies that participate in the notified IPCEI Microelectronics and will benefit from Member States support, are:

(a) 3D-Micromac AG ("3D-Micromac")

3D-Micromac is a supplier of laser micromachining systems. In addition, 3D-Micromac offers coating and printing technologies combined with laser processes. 3D-Micromac focuses on end-customer business in five markets; medical technology, photovoltaics, semiconductor, glass and display as well as micro diagnostics.

(b) Advanced Mask Technology Center GmbH & Co. KG, Rähnitzer ("AMTC")

AMTC manufactures photomasks (for 193 nm dry and immersion lithography as well as for EUV lithography).

(c) AP&S International GmbH ("AP&S")

AP&S acts in the field of "wet-chemistry based wafer processing equipment" for the semiconductor and MEMS Industry. The company designs and manufactures processing custom tailored tools for wafer sizes

up to 300 mm diameter while tool layout, type of automation and software solutions are in line with the specific requirements of each customer.

(d) AZUR SPACE Solar Power GmbH (“AZUR SPACE”)

Business domains of AZUR SPACE are optoelectronic devices for light emission and detection and optical power transmission in infrared spectral region, GaN field effect transistor structures for power applications as well as high efficiency III/V (boron group/nitrogen group) based multi-junction solar cells for space and terrestrial concentrator applications.

(e) Carl Zeiss SMT GmbH and Carl Zeiss Oberkochen Grundstücks GmbH & Co.KG (“Zeiss”)

Zeiss supplies the semiconductor industry with edge optical projection systems, and mask metrology, defect inspection and mask repair equipment. Furthermore, Zeiss SMT provides various producers of semiconductor manufacturing equipment with optical sub-systems and components.

(f) Cologne Chip AG (“Cologne Chip”)

Cologne Chip is a fabless semiconductor manufacturer based in Germany. For more than 20 years the company has developed and merchandised transceiver ICs for digital telecommunications. Besides, building blocks for IC designs – the so called IP blocks - are offered for licensing. As a new product segment, Cologne Chip is about to bring Europe's first FPGA chip to the market.

(g) CorTec GmbH (“CorTec”)

CorTec, an SME with about 40 employees, is active in the field of implantable medical devices and will establish a new facility, including cleanroom and micro-machining equipment in Freiburg, Germany, for the FID of MEMS-based sensor arrays for electrical interaction with neural tissue.

(h) Elmos Semiconductor AG (“Elmos”)

Elmos is a developer and manufacturer of semiconductor-based system solutions. The core competency of Elmos is the development, production, and sale of mixed-signal semiconductors, involving sensors and MEMS.

(i) GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG (“Globalfoundries” or “GF”)

Globalfoundries is a semiconductor foundry with manufacturing sites in Europe, USA and Asia. Globalfoundries Fab 1 in Dresden, Germany serves customers with innovative semiconductor products in 28 nm, 32 nm and 40 nm technologies on 300 mm wafers.

(j) Infineon Technologies AG and Infineon Technologies Dresden GmbH (“Infineon”)

Infineon designs, develops, manufactures and markets semiconductors and system solutions. The focus of its activities is on automotive electronics, industrial electronics, RF applications, mobile devices and hardware-based security.

(k) Integrated Compound Semiconductors Ltd ("ICS")

The company specialises in design and manufacture of compound semiconductor RF and optical devices. It supplies both wafer format and fully packaged components.

(l) IQE plc ("IQE")

The company provides pure-play foundry services for advanced compound semiconductor wafers.

(m) Murata Integrated Passive Solutions ("Murata")

Formerly IPDiA, the company has been acquired by Murata in October 2016 and became Murata Integrated Passive Solutions in April 2017. Murata's innovative silicon Integrated Passive Devices technology enables silicon passive components for specific markets where high performance and miniaturization are required (for example implantable and wearable medical electronics, high reliability, and telecommunications).

(n) Newport Wafer Fab Limited (also "NWF")

Newport Wafer Fab is an open-access integrated silicon, and compound-on-silicon wafer fab providing manufacturing services.

(o) OSRAM Opto Semiconductors GmbH ("OSRAM")

The major activities of OSRAM Opto Semiconductors GmbH are focused on visible and infrared light-emitting diodes (LEDs) and power lasers. The company develops technologies for illumination, visualization and sensing. OSRAM Opto Semiconductors has full, in-house production capabilities consisting of facilities for epitaxy, chip processing, light conversion technologies and device packaging.

(p) Racyics GmbH ("Racyics")

Racyics is a System-on-Chip design service provider with focus on advanced semiconductor nodes. The company offers a wide range of design services including custom IP and turnkey SoC solutions.

(q) Robert Bosch GmbH and Robert Bosch Semiconductor Manufacturing Dresden GmbH ("Bosch")

Bosch is a supplier of technology and services, active in four business sectors: Mobility Solutions, Industrial Technology, Consumer Goods, and Energy and Building Technology. Robert Bosch Semiconductor Manufacturing Dresden GmbH is a 100% subsidiary of Robert Bosch GmbH and part of the Automotive Electronics (AE) division, as one division of Mobility Solutions.

(r) SEMIKRON Elektronik GmbH & Co. KG ("SEMIKRON")

SEMIKRON is a supplier of power electronic chips, modules, components and systems in the power range from approx. 10 kW up to several MWs.

(s) Sofradir SAS ("Sofradir")

Sofradir is active in high-performance infrared (IR) imaging solutions for military, space and industrial markets. Sofradir pioneers developments in high performance IR detectors based on sophisticated technologies: Mercury Cadmium Telluride (MCT), Indium Antimonide (InSb), Quantum Well Infrared Photodetectors (QWIP), Indium Gallium Arsenide (InGaAs), and a-Si Micro-bolometers.

(t) Soitec SA ("Soitec")

Soitec designs and manufactures innovative semiconductor materials. Soitec offers solutions for miniaturizing chips, improving their performance and reducing their energy usage. Its products are used to manufacture chips that go into smart phones, tablets, computers, IT servers and data centers as well as electronic components in cars, connected devices, and industrial and medical equipment.

(u) SPTS Technologies Limited ("SPTS")

The company is a supplier of advanced wafer processing equipment to device manufacturers.

(v) ST Microelectronics SA (also "ST France")

ST France is established from several sites with around 10 000 employees dedicated to Research & Development, product design, manufacturing (Front End and Back End), tests (EWS), sales and marketing. R&D is carried out on various sites: Crolles, Grenoble, Tours, Rousset, Rennes, with some complementary R&D activities on other French sites (Le Mans, Sophia, Paris).

(w) ST Microelectronics S.r.l. (also "ST Italy")

ST Italy is the most important semiconductor company in Italy. ST counted 10,178 employees at the end of 2017. ST Italy has premises located in different sites, with wafer fabs, business offices and R&D laboratories.

(x) TDK-Micronas GmbH ("TDK-Micronas" or "TDK")

TDK-Micronas offers Hall sensors for both the Automotive and the Industrial market.

(y) ULIS SAS ("ULIS")

ULIS is specialized in developing, manufacturing, and marketing innovative thermal image and thermal activity sensors enabling them to offer products with specialised advantages.

(z) X-FAB Dresden GmbH & Co. KG and X-Fab MEMS Foundry GmbH ("X-FAB Germany" of "X-FAB DE")

X-FAB DE belongs to the specialty foundry group of X-FAB for analogue/mixed-signal semiconductor technologies, providing manufacturing and design support services for customers that design analogue/mixed-signal integrated circuits (ICs) and other semiconductor devices (e.g. MEMS) for use in their own products or the products of their customers. X-FAB DE creates customized analogue/mixed-signal ICs and other semiconductor devices for use in a variety of applications with a focus on the automotive, industrial and medical device end-user markets.

(aa) X-FAB France SAS ("X-FAB France" or "X-FAB FR")

X-FAB France is part of the X-FAB group since 2 years. The company is manufacturing semiconductors at Corbeil-Essonne (France) since many years. X-FAB France creates customized analog/mixed-signal ICs and other semiconductor devices for use in a variety of applications with a strategic focus on the automotive, industrial, medical and communication device end-user markets.

(249) France and Italy submit that two research organisations will take part in the IPCEI Microelectronics projects and activities as partners; however, due to their research organisation status and performance of non-economic activities, and the fact that their economic activities comply with the ancillarity principle as defined by point 20 of the R&D&I Framework[28], these research organisations shall not be considered as beneficiaries of aid:

(a) CEA-LETI

Leti, a technology research institute at CEA (*Commissariat à l'énergie atomique et aux énergies alternatives*), pioneers micro technologies, tailoring differentiating applicative solutions for a wide range of markets. The institute tackles critical challenges such as healthcare, energy, transport and ICTs.

(b) Fondazione Bruno Kessler ("FBK")

FBK is a Research Foundation that conducts scientific research in the areas of Information and Communication Technology, Advanced Materials and Microsystems, Theoretical and Nuclear Physics and Mathematics Research. FBK Micro-Nano characterization and fabrication Facility (MNF) offers a combination of silicon process and characterization capabilities supported by state-of-the-art processing and analytical equipment. The core business is Si technology of IC and MEMS and materials characterization and analysis.

[28] COMMUNICATION FROM THE COMMISSION - Framework for State aid for research and development and innovation, OJ C 198 of 27.06.2014, p. 1

(250) The Member States submit amounts of the State aid under the measures that will be provided to the beneficiaries, together with the individual eligible costs and funding gaps:

Germany	Eligible costs			Funding gap	Aid amounts	
	R&D	FID	Total		Nominal	Net present value ("NPV")
3D-Micromac	*[…]*	*[…]*	*[1,300 - 4,800]*	*[2,000 - 5,500]*	*[1,100 - 4,600]*	*[0,500 - 4,000]*
AMTC	*[…]*	*[…]*	*[40,000-55,000]*	*[60,000-80,000]*	*[45,000-60,000]*	*[40,000-55,000]*
AP&S	*[…]*	*[…]*	*[5,000-10,000]*	*[5,000-10,000]*	*[0,500-4,000]*	*[0,500-4,000]*
AZUR SPACE	*[…]*	*[…]*	*[30,000-40,000]*	*[5,000-10,000]*	*[5,000-10,000]*	*[5,000-10,000]*
Carl Zeiss	*[…]*	*[…]*	*[300,000-425,000]*	*[305,000-430,000]*	*[65,000-90,000]*	*[60,000-85,000]*
Cologne Chip	*[…]*	*[…]*	*[5,000-13,500]*	*[5,000-10,000]*	*[2,000-5,500]*	*[1,500-5,000]*
CorTec	*[…]*	*[…]*	*[0,100-3,600]*	*[0,100-3,600]*	*[0,001-3,600]*	*[0,001-3,600]*
Elmos	*[…]*	*[…]*	*[30,000-40,000]*	*[17,000-25,500]*	*[12,500-20,000]*	*[12,500-20,000]*
Globalfoundries	*[…]*	*[…]*	*[280,000-405,000]*	*[320,000-445,000]*	*[200,000-325,000]*	*[200,000-265,000]*
Infineon	*[…]*	*[…]*	*[190,000-252,000]*	*[220,000-345,000]*	*[100,000-160,000]*	*[80,000-95,000]*
OSRAM	*[…]*	*[…]*	*[80,000-105,000]*	*[80,000-105,000]*	*[60,000-80,000]*	*[50,000-65,000]*
RacyICs	*[…]*	*[…]*	*[0,100-3,600]*	*[0,100-3,600]*	*[0,100-3,600]*	*[0,100-3,600]*
Bosch	*[…]*	*[…]*	*[425,000-550,000]*	*[190,000-252,000]*	*[190,000-252,000]*	*[150,000-212,000]*
SEMIKRON	*[…]*	*[…]*	*[45,000-60,000]*	*[18,000-28,000]*	*[12,000-20,500]*	*[10,000-18,500]*
TDK-Micronas	*[…]*	*[…]*	*[35,000-50,000]*	*[18,000-28,000]*	*[12,000-20,500]*	*[12,000-20,500]*
X-FAB (DE)	*[…]*	*[…]*	*[55,000-75,000]*	*[75,000-100,000]*	*[70,000-95,000]*	*[60,000-80,000]*
Sum	*[…]*	*[…]*	**1,450,023**			

Table 3: German State aid per company (in 1000€, estimated)

France	Eligible costs			Funding Gap	Aid amount	
	R&D	FID	Total		Nominal	NPV
Murata	*[…]*	*[…]*	*[35,000-45,000]*	*[10,000-18,500]*	*[5,000-12,000]*	*[8,000-15,000]*
Sofradir	*[…]*	*[…]*	*[32,000-42,000]*	*[6,000-11,000]*	*[5,000-10,000]*	*[5,000-10,000]*
Soitec	*[…]*	*[…]*	*[200,000-325,000]*	*[70,000-90,000]*	*[85,000-110,000]*	*[60,000-80,000]*
ST-France	*[…]*	*[…]*	*[1,200,000-1,575,000]*	*[200,500-262,500]*	*[200,500-325,500]*	*[188,000-250,000]*
ULIS	*[…]*	*[…]*	*[60,000-80,000]*	*[15,000-23,500]*	*[11,500-20,000]*	*[10,000-18,500]*
X-Fab (FR)	*[…]*	*[…]*	*[68,500-78,500]*	*[12,500-21,000]*	*[14,500-23,000]*	*[10,500-19,000]*
Sum	*[…]*	*[…]*	**1,998,715**			

Table 4: French State aid per company (in 1000€, estimated)

UK	Eligible costs			Funding Gap	Aid amount[29]
	R&D	FID	Total		
ICS	*[…]*	*[…]*	*[5,000-10,000]*	*[5,000-10,000]*	*[5,000-10,000]*
IQE	*[…]*	*[…]*	*[30,000-40,000]*	*[15,000-23,500]*	*[10,000-18,500]*
Newport Wafer Fab	*[…]*	*[…]*	*[35,000-45,000]*	*[12,000-20,500]*	*[7,500-16,000]*
SPTS	*[…]*	*[…]*	*[45,000-60,000]*	*[5,000-10,000]*	*[4,000-9,000]*
Sum	*[…]*	*[…]*	**143,801**		

Table 5: UK State aid per company (in 1000 €, estimated)

Italy	Eligible costs			Funding Gap	Aid amount	
	R&D	FID	Total		Nominal	NPV
ST-Italy	*[…]*	*[…]*	*[1,950,000-2,515,000]*	*[420,000-550,000]*	[*600,000-850,000*]	[*420,000-550,000*]

[29] According to the UK authorities, the aid could reach up to 100% of funding gap. However, *[…]* there is no restriction on the aid instrument intended for support (also see recital (256) below).

Sum	*[…]*	*[…]*	***[1,950,000-2,515,000]***			

Table 6: Italian State aid per company (in 1000€, estimated)

(251) The Member States submit that the durations of the individual projects of the participating companies and ROs differ. The activities' start is in the period between January 2017 and January 2019, and in any case not before the companies made their request for support to the public authorities.

(252) The funding period (i.e. the period during which the costs, which the companies can claim to be eligible, should be incurred) is the following:

(a) For Germany: *[...]*, and the German authorities have indicated that eligible costs will be funded only under the condition of approval of the IPCEI Microelectronics by the European Commission;

(b) For France: *[...]* and the funding will be effectively paid only after European Commission approval;

(c) For Italy: *[...]*;

(d) For the UK: *[...]*.

2.7.4. The aid instruments

(253) The aid to be granted by the German authorities will take the form of grants.

(254) The aid to be granted by the French authorities will take the form of grants and, for one beneficiary, *[...]*, of a combination of a grant and a loan. The French authorities indicated that contract negotiations on the loan are ongoing, but they have committed that in any case the aid amount to *[...]*, calculated in terms of Gross Grant Equivalent of the loan and the grant's net present value, will remain within the notified aid amount.

(255) The form of aid to be granted by the Italian authorities will take the form of grants, according to the information in the notification.

(256) The UK authorities indicate that *[...]* there is no restriction on the aid instrument intended for support and they consider that to share the risk, a range of support instruments will be appropriate. These are expected to include both loans and grants.

2.8. Granting of the aid under the notified measures

(257) The effective implementation of State aid by the national authorities is subject to the prior approval of the European Commission.

2.9. Transparency

(258) The Member States have in their notification committed to respect the transparency and publication requirements of points 45 and 46 of the IPCEI Communication.

3. ASSESSMENT OF THE MEASURES

3.1. Presence of State aid pursuant to Article 107 (1) TFEU

(259) According to Article 107(1) TFEU, "any aid granted by a Member State or through State resources in any form whatsoever which distorts or threatens to distort competition by favouring certain undertakings or the production of certain goods shall, in so far as it affects trade between Member States, be incompatible with the internal market".

(260) In order to qualify as State aid under Article 107(1) TFEU, the following cumulative conditions must be met: (i) the measure must be imputable to the State and financed through State resources; (ii) it must confer an advantage on its recipient; (iii) that advantage must be selective; and (iv) the measure must distort or threaten to distort competition and affect trade between Member States.

(261) The public support measures of France, Germany and Italy will be financed with funds stemming from the respective State budgets; in addition, the French authorities point out that funds stemming from the local authorities will be used for the financing. The UK authorities point out that all sources for support will be considered including support from national, regional and sub-regional authorities or State resources in the UK. The measures therefore involve State resources. The aid will be granted by the Direction General for Enterprise in France, by the Federal Ministry for Economic Affairs and Energy in Germany, by the Ministry of Economic Development in Italy and by the Welsh Government in the UK. Thus, the aid is imputable to the relevant States.

(262) The Member States only grant support to the beneficiaries listed in recital (248) above and the funding is not available to all undertakings in a comparable situation. By contributing to the financing of the R&D&I and FID activities of the selected firms with funds that would not have been available under normal market conditions, the measures give the aid beneficiaries a selective economic advantage.

(263) The aid beneficiaries operate in the industry sectors in the technology fields, as described above. These are economic sectors open to intra-EU trade (both in terms of supply and demand). Therefore, the measures may affect trade between Member States.

(264) By reinforcing the aid beneficiaries' position in their respective sectors, the measures are therefore liable to distort competition by putting the beneficiaries at a competitive advantage as compared to their competitors.

(265) In the light of the foregoing, the Commission considers that the public resources granted to the aid beneficiaries in the form of grants and loans for the R&D&I and FID activities as described within the framework of this IPCEI Microelectronics project qualify as State aid within the meaning of Article 107(1) TFEU.

3.2. Legality of the aid measures

(266) By notifying the measures before putting them into effect, the German, French, Italian and the UK authorities have fulfilled their obligations under Article 108(3) TFEU.

3.3. Assessment of the aid measures

3.3.1. Applicable legal basis for assessment

(267) In derogation from the general prohibition of State aid laid down in Article 107(1) TFEU, aid may be declared compatible by the Commission if it can benefit from one of the derogations enumerated in Article 107(2) and (3) TFEU.

(268) According to Article 107(3)(b) TFEU, aid to promote the execution of an important project of common European interest may be considered to be compatible with the internal market.

(269) In the IPCEI Communication, the Commission has provided guidance on the analysis of the compatibility with the internal market of State aid to promote the execution of important projects of common European interest. The criteria set out in the IPCEI Communication are applicable to this case.

(270) As Article 107(3)(b) TFEU allows the Commission to consider as compatible with the internal market aid to promote the execution of an important project of common European interest, it is appropriate to consider first whether the notified measures relate to such a project. These general eligibility criteria are assessed in section 3.3.2. Second, it needs to be considered whether the criteria for declaring the aid compatible with the internal market are met. The compatibility criteria are assessed in section 3.3.3.

3.3.2. General eligibility criteria

(271) In order to be eligible for aid under Article 107(3)(b) TFEU, the notified measures must involve a project, the project must be of common European interest, and the project must be important. These three criteria are considered below.

3.3.2.1. Definition of a project

(272) Point 12 of the IPCEI Communication requires that the aid proposal concerns a single project which is clearly defined in respect of its objectives as well as the terms of its implementation, including its participants and its funding.

(273) According to point 13 of the IPCEI Communication, the Commission may also consider eligible an "integrated project", that is to say, a group of single projects inserted in a common structure, roadmap or programme aiming at the same objective and based on a coherent systemic approach. The individual components of the integrated project may relate to separate levels of the supply chain but must be complementary and necessary for the achievement of the important European objective.

(274) The participating Member States consider the notified IPCEI Microelectronics to constitute an integrated project. The Commission shares this analysis for the reasons explained below.

(275) The Commission finds that the IPCEI Microelectronics is designed in such a way as to contribute to a common objective, formulated by the participating Member states and companies, as described in recitals (11), (12) and (13) above. The overall objective of the proposed IPCEI Microelectronics is to be reached by combining R&D&I and FID activities in five technology fields, which constitute the individual but interlinked components of the IPCEI Microelectronics. As described in section 2.4 above, each technology field is complementary to the others and necessary for the achievement of the overall IPCEI Microelectronics objective. For example, achieving the specific objective of the first technology field, i.e. advance the energy efficiency of chips, is "necessary for the overall objective of the IPCEI Microelectronics because the urgency of improved energy efficiency cuts across all technology fields and downstream ICT markets and applications" (see recital (110) above). Work within the first technology field will enable energy-efficient technologies for data processing, data collection and data communication in electronic systems, which also include power devices (technology field 2), sensors (technology field 3), lithography equipment enhancements (technology field 4) and compound semiconductors for example in the case of data centres (technology field 5). As described in recitals (27) to (122) above, the technology fields are inserted in a common structure and roadmap, and based on a coherent systemic approach.

(276) In order to ensure the coherent implementation of the IPCEI Microelectronics, the participating Member States will establish a common governance structure[30], as described in section 2.3, under a Supervisory Board (SB), which will have the task to review the progress and the results of the project and propose changes if necessary, giving specific attention to the benefit for the European society. The Commission will be represented in the SB with a delegate.

(277) Therefore, the Commission concludes that the notified IPCEI Microelectronics qualifies as an integrated project in the meaning of the Communication, as its individual TFs components are inserted in a common structure and roadmap, and aim at the same objective, being complementary and necessary for the achievement of the important common European objective.

3.3.2.2. Common European interest

(278) In order to establish that a project qualifies as being of common European interest, the IPCEI Communication sets out general cumulative criteria (section (a) below) as well as general positive indicators (section (b) below). In addition, the IPCEI Communication specifies certain criteria depending on the type of the project (section (c) below).

[30] The Commission notes that all actions of the governance must comply with the EU rules on competition law.

(a) General cumulative criteria

(279) Firstly, according to point 14 of the IPCEI Communication, the project must contribute in a concrete, clear and identifiable manner to one or more Union objectives and must have a significant impact on the competitiveness of the Union, sustainable growth, addressing societal challenges or value creation across the Union.

(280) According to point 15 of the IPCEI Communication, the project must represent an important contribution to the Union's objectives, for instance by being of major importance for one of the strategies or policies listed, which explicitly include the European strategy for KETs and the Electronics Strategy for Europe, the Europe 2020 strategy, the Union's flagship initiatives such as the Innovation Union, Digital Agenda for Europe, and the Integrated Industrial Policy for the Globalisation Era.

(281) The Commission considers the IPCEI Microelectronics of major importance for Europe's Electronics Strategy. In its Communication on Electronics Strategy for Europe[31], the Commission highlights that "Micro- and nanoelectronic components and systems are not only essential to digital products and services; they also underpin innovation and competitiveness of all major economic sectors". Furthermore, this Strategy underlines the importance of microelectronics in addressing societal challenges: "Micro- and nanoelectronics are not only the computing power in PCs and mobile devices. They fulfil also the sensing and actuating functions found for example in smart meters and smart grids for lower energy consumption, or in implants and sophisticated medical equipment for better healthcare and for helping the elderly population. They are also the building blocks for better security, for the safety and efficiency of the whole transport systems and for environmental monitoring". This IPCEI covers the two essential dimensions of microelectronics, namely the “More Moore” track "aiming at higher performance, lower costs and less energy consumption", and the “More-than-Moore” track that "is at the basis of innovations in many important fields such as energy-efficient buildings, smart cities and intelligent transport systems". Furthermore, it covers those two essential dimensions extensively by innovative solutions to digital and RF components, power electronic components, sensors, production processes, and photonics components, beyond their current state of the art. Therefore the Commission considers that the IPCEI Microelectronics provides a major contribution to the Electronics Strategy for Europe.

(282) The Commission furthermore notes that the preparation of this IPCEI was deemed "of particular importance" in the Strategy for Digitising European Industry[32].

(283) The Commission considers the IPCEI Microelectronics of major importance for the European strategy for KETs[33]. Microelectronics is recognised by the

[31] COM(2013)298 A European Strategy for Micro- and Nanoelectronic Components and Systems.

[32] Cf. COM(2016) 180 final of 19.4.2016.

[33] COM(2012) 341 final of 26.6.2012 – 'A European strategy for Key Enabling Technologies – A bridge to growth and jobs’.

Commission as one of the Key Enabling Technologies. The Communication on KETs identifies microelectronics as a KET that is defined as ‘knowledge intensive and associated with high R&D intensity, rapid innovation cycles, high capital expenditure and highly skilled employment. They enable process, goods and service innovation throughout the economy and are of systemic relevance. They are multidisciplinary, cutting across many technology areas with a trend towards convergence and integration". The IPCEI Microelectronics contains high R&D intensity as demonstrated in section 3.3.2.2 c). The different technology fields of this IPCEI cover a wide range of multidisciplinary technologies cutting across many areas as demonstrated by the integrated nature of the project (section 2.4). The innovations resulting from breakthrough technologies are further translated into new products, processes and services through the IPCEI Microelectronics' first industrial deployments. The generated innovations will be tested during the IPCEI Microelectronics to be taken up by the wider economy once mature enough after the end of the project. The Communication also indicates that "microelectronics is of systemic relevance to the EU’s capability to innovate and modernise its industrial base". The fact that the Commission has recognised microelectronics as a KET signifies that strengthening Europe's ability to develop microelectronics "plays an important role in contributing to sustainable competitiveness and growth".

(284) In its document "Europe 2020, a strategy for smart, sustainable and inclusive growth", the European Commission proposes a response to "Europe’s innovation gap". The Commission shares the Member States' view that the notified IPCEI Microelectronics directly supports this goal by providing the building blocks for new products and services which become available and affordable for the downstream markets and population at large. Microelectronic components and systems enable the development of innovative technologies across sectors to address societal needs in Europe. As described above in sections 2.2 and 2.6, the activities in this IPCEI are innovative and will lead to innovative microelectronics components and systems, which, in turn, drive innovation in the downstream markets.

(285) In addition, the Commission considers that the IPCEI Microelectronics will also have a significant impact on sustainable growth, addressing societal challenges and value creation across the Union by enabling the emergence of new downstream markets in Europe, in particular the Internet of Things.

(286) In its Communication on a Strategic Energy Technology Plan[34], the Commission calls for "bringing together energy and information and communication technology researchers and companies to support the development of innovative solutions and, over time, encourage the integration of these services into smart homes with other digitally delivered services, such as environmental control, electro mobility and e-health via the Internet of Things". This IPCEI will provide essential technologies supporting this integration through power electronic components, low power components for local data processing, as well as sensors.

[34] C(2015)6317 – ‘Towards an Integrated Strategic Energy Technology (SET) Plan: Accelerating the European Energy System Transformation’

(287) The Commission Strategy on Low-Emission Mobility[35] recognizes that "the widest range of options is currently available for passenger cars and buses, and solutions are rather straightforward for rail through electrification". At the same time it clarifies that "in order to achieve mass acceptance and deployment of electric vehicles, charging and maintenance infrastructure needs to become widely available throughout Europe", with direct implication for the uptake of electric vehicles in Europe. For any of the alternative fuels for the future low-emission vehicles, electrification is a necessary means, either in the vehicle for power train control or in electric refuelling infrastructures. This IPCEI will deliver a wide set of components from power electronics to sensors and computing capacity with the aim to enable the downstream innovation in engineering alternative fuel and electric vehicles, essential to achieve low emission mobility in Europe, contributing to air quality targets[36].

(288) Also in view of the high number and significance of the R&D&I and first industrial deployment activities in microelectronics that will be carried out in this IPCEI and the high related investments that will be made, the Commission considers that the IPCEI Microelectronics represents an important contribution to the Union's objectives.

(289) Furthermore, it is the view of the Commission, as highlighted by the final KETs report, and the EU's strategy announced by vice President Kroes in 2014[37] and Commissioner Oettinger in 2015[38], that the importance of microelectronics in Europe goes far beyond the prospects of the sector due to its cross-cutting character.

(290) Based on the foregoing, the Commission concludes that the IPCEI microelectronics contributes in a concrete, clear and identifiable manner to one or more Union objectives and has a significant impact on the competitiveness of the Union, sustainable growth, addressing societal challenges or value creation across the Union.

(291) Secondly, the IPCEI Communication, point 16, further requires that more than one Member State is involved. The notified IPCEI Microelectronics involves four Member States, Germany, France, the UK, and Italy.

(292) Thirdly, as required by points 16 and 17 of the IPCEI Communication, an IPCEI must benefit the European economy or society via positive spillover effects. According to the IPCEI Communication, "The benefits of the project must be clearly defined in a concrete and identifiable manner" and "The benefits of the project must not be limited to the undertakings or to the sector concerned but must be of wider relevance and application to the European economy or society through positive spillover effects (such as having systemic effects on multiple levels of the value chain, or up- or downstream markets, or having alternative

[35] COM(2016)501 – 'A European Strategy for Low-Emission Mobility'

[36] COM(2018) 330 final – 'A Europe that protects: Clean air for all'

[37] Speech at IMEC Technology Forum, Leuven, 4 June 2014.

[38] Keynote speech at the Design, Automation and Test in Europe Conference (DATE), Grenoble, 10 March 2015.

uses in other sectors or modal shift) which are clearly defined in a concrete and identifiable manner."

(293) The IPCEI Communication requires for spillover effects to be identified at all the following levels: beyond the participating Member States ("European economy or society"); beyond the aid beneficiaries ("not be limited to the undertakings"); beyond the sector(s) in which the aid beneficiaries are active ("… or to the sector concerned").

(294) Insofar as the IPCEI Communication allows higher aid intensities and a wider scope of eligible costs for activities, including FID which is not covered by the R&D&I State aid rules, the efforts required under the IPCEI Communication should in principle go further than those required under the general R&D&I rules. Furthermore, spillover effects should be generated not only by the R&D&I activities, but also by the FID activities, especially given that an important part of the funding in this IPCEI flows to FID.

(295) The Commission recognizes that the overall objective of the IPCEI Microelectronics is to develop innovative technologies and components for Automotive, IoT and other key applications and to establish first industrial deployment in these fields, in order to unlock the full technological and economic potential of the Key Enabling Technology (KET) microelectronics and to transfer it to European existing and new downstream industries for new or improved applications as well as new R&D.

(296) In addition, the participants to this IPCEI will undertake actions in order to spillover the benefits generated by this IPCEI.

(297) The Commission takes note of the actions that the participating companies and the IPCEI Microelectronics governing bodies will undertake on dissemination of knowledge and results generated in the IPCEI Microelectronics (as described in sections 2.5.1 to 2.5.6), for spillover effects generated in FID (described in section 2.5.7) and for spillover effects in downstream markets (see section 2.5.8). The Commission notes, as described in recitals (94) to (98) above, the set up of the annual IPCEI Microelectronics conference, to inform the interested expert community on the R&D progress and the technical results of the IPCEI Microelectronics, and the set up of the IPCEI Microelectronics website, which will serve as a dissemination channel and will list all spillover activities to which the individual IPCEI partners have committed themselves.

(298) Moreover, Member States have ensured that certain companies, having regard of their position on the market, will undertake additional reinforced individual spillover actions (see recitals (363) to (367) below).

(299) Thus, based on the combination of the spillovers at the level of the IPCEI Microelectronics with the ones at individual companies' level, and covering the spillovers targeted at the dissemination of the IPCEI Microelectronics-related results in the areas of non-IPR protected knowledge, IPR-protected knowledge and FID, the Commission considers that the IPCEI's benefits will be of wider relevance to the European economy or society, therefore this eligibility condition is deemed to be satisfied.

(300) Fourthly, as required by point 18 of the IPCEI Communication, co-financing of the beneficiaries is present, as evidenced by the fact that aid to individual beneficiaries does not cover 100% of the individual projects' costs.

(301) Fifthly, the public funding of the IPCEI Microelectronics does not relate to environmentally harmful subsidies, therefore it is not in conflict with the principle of phasing out such subsidies, as required by point 19 of the IPCEI Communication.

(302) Based on the above considerations, the Commission considers the general cumulative criteria for eligibility of the notified IPCEI microelectronics to be met.

(b) General positive indicators

(303) All Member States where a semiconductor industry is active were made aware of the creation of the IPCEI Microelectronics at the onset of the project. The Commission facilitated the emergence of the project[39]. The governance structure of the project involves the Commission through participation into the Supervisory Board. Finally, as described above, the project involves important collaborative interactions in terms of number of partners, involvement of organisations of different sectors and the involvement of undertakings of different sizes.

(304) In its assessment of the eligibility of the IPCEI Microelectronics, on grounds of section 3.2.2. of the IPCEI Communication, the Commission therefore takes note of the above-described general positive indicators.

(c) Specific criteria

(305) Point 21 of the IPCEI Communication provides that R&D&I projects must be of a major innovative nature or constitute an important added value in terms of R&D&I in the light of the state of the art in the sector concerned. According to point 22 of the IPCEI Communication, projects comprising of industrial deployment must allow for the development of a new product or service with high research and innovation content and/or the deployment of a fundamentally innovative production process. Regular upgrades without an innovative dimension of existing facilities and the development of newer versions of existing products do not qualify as IPCEI.

(306) Based on the information provided by the notifying Member States (see section 2.6 above), the Commission's assessment confirms that the R&D&I activities carried out in each of the technology fields clearly aim to result in outcomes that will bring the technology development in the relevant technology field beyond the current state-of-the art.

(a) In particular, the R&D&I activities in TF1 aim to achieve major innovation on new variants of FDSOI unlocking applications requiring low and ultra-low

[39] In particular, the European Commissioner for Digital Agenda met the industry involved in setting up the IPCEI Microelectronics twice at two roundtables, one at Cebit in Hannover on 16/03/2016 and another time on 24/11/2016 at the occasion of the European Nanoelectronics Forum in Rome.

power, including through the implementation of innovative system-on-chip and FPGA circuits as well as new embedded memories.

(b) The R&D&I activities in TF2 aim to create a major advancement in bringing innovative technologies in the power and radio-frequency components, including with substantial gains in power losses, packaging, cooling capability and durability, as well as in smart power components with deeply enhanced power controlling capacity.

(c) The R&D&I activities in TF3 aim to ensure the emergence of innovative components for sensing a wide range of parameters including magnetic, pressure, sound, imaging in infrared in various spectral ranges, spatial and ranging, chemical, while bringing further innovation in the packaging of those sensors therefore substantially increasing their capacity. The R&D&I activities in this TF will also innovate in the co-integration of those sensors with electronics while tackling the essential issue of security and safety, to unlock a wider introduction of sensors in many application areas.

(d) The R&D&I activities in TF4 aim to enable the next generation of EUV lithography *[...]* and the necessary accompanying technology to design the related masks. This will be complemented by the introduction of a new technology for enhancing *[...]* on lithography mask, in DUV and EUV technologies.

(e) The R&D&I activities in TF5 aim to cross a gap in terms of the quality and wafer diameter of epitaxial wafers for compound semiconductors that will unlock a wide range of applications currently not addressable. It is aimed to achieve this through innovation in the area of materials and components for light-emitting diodes, integrated photonics, infrared imaging, ultraviolet sensing, radio-frequency components as well as silicon photonics.

(307) As evidenced by the alternative scenarios for the advancement of the constituent technology fields, as submitted by the Member States, much more modest R&D&I activities (in terms of their scope) would have been pursued in these fields in the absence of public support to the notified IPCEI Microelectronics. Any such advancements would also have taken longer time without the aid.

(308) As regards the FID activities carried out in the technology fields, the Commission considers that it has been sufficiently demonstrated by the notifying Member States that these allow for the development of new products with high research and innovation content and the deployment of fundamentally innovative production processes.

(a) In particular, the FID activities in TF1 allow for the development of innovative substrates, low power components with a large number of essential technology variants to address battery-less applications, connectivity including multi-standard radios, harsh environments, as well as configurable components (new products with high research and innovation content) and the deployment of fundamentally innovative production processes for the deployment of innovative substrates and the behavioural analysis of (ultra-)low power components.

(b) The FID activities in TF2 allow for the development of mixed signal high voltage and high power components covering a large range from medium to high voltages, silicon and III-V power electronics and III-V power radiofrequency components, including cooling functionality, integrated passive components for power applications, along with the accompanying functionalities for safety critical applications, power supply regulation, motor control, sensor interfaces (new products with high research and innovation content) and the deployment of fundamentally innovative production processes for wafer singulation, for advanced innovative packages for robustness increase for harsh environments, substantial heat dissipation increase and 3D integration, for high current handling and high voltage isolation.

(c) The FID activities in TF3 allow for the development of a wearable neuromodulation-based therapeutic system, single photon avalanche diode arrays, monolithic integrated thermopile arrays, gesture recognition system, high-speed ultrasonic sensors, automotive short- and long-range radar sensors, millimetre wave integrated radars, highly sensitive magnetic sensors, advanced integrated microphones, high performance 6-axis inertial sensors, small high performance pressure sensors, advanced CMOS image sensors and vision systems, microbolometer focal plane arrays, microsystems with advanced actuation (new products with high research and innovation content) and the deployment of fundamentally innovative production processes for advanced innovation packages including hermetic and low pressure packaging, millimetre wave, multi-chip integration, specific decoupling and protection of the sensors against the disturbances from their environments, for highly controlled material composition and new functional material integration, for assembly technologies for safety critical applications, for transfer printing.

(d) The FID activities in TF4 allow for the development of *[...]* extreme ultraviolet optics system and related reflective lithography mask (new products with high research and innovation content) and the deployment of fundamentally innovative production processes for extreme accuracy of highly non-spherical reflective mirrors at extreme ultraviolet, fabrication of extreme ultraviolet masks *[...]*, inspection and repair tools for optics and masks, advanced optical correction *[...]* and extreme ultraviolet lithography masks.

(e) The FID activities in TF5 allow for the development of infrared focal plane arrays, analogue high-speed circuits and photonic components, photodiodes for power by light, 2D LED arrays, UV LEDs, semiconductor lasers (new products with high research and innovation content) and the deployment of fundamentally innovative production processes for 3D integration of photonic components with their control electronics, for advanced substrates and compound semiconductor processing for high-speed electronic and photonic components.

(309) Based on the foregoing, the Commission considers that the specific criteria established by the IPCEI Communication in points 21 and 22 as regards the R&D&I content of the research projects and FID projects that will be performed

within the framework of the technology fields of the IPCEI Microelectronics are fulfilled.

3.3.2.3. Importance of the project

(310) According to section 3.3 of the IPCEI Communication, in order to qualify as an IPCEI, a project must be important quantitatively or qualitatively. It should either be particularly large in size or scope and/or imply a very considerable level of technological or financial risk.

(311) As evidenced by the number of participating companies (29 partners and 370 indirect partners), the amount of total investments (over EUR 7.8 billion) and the amounts of State aid (see recital (250) above) envisaged for the project, and the innovative character of the technologies concerned (as described in section 2.6), the Commission considers the IPCEI Microelectronics an important project within the requirement of point 3.3. of the IPCEI Communication.

3.3.2.4. Conclusion on the eligibility of the project

(312) As demonstrated in the recitals from (272) to (311) above, the general eligibility criteria are met by the IPCEI Microelectronics.

3.3.3. Compatibility criteria

(313) When assessing the compatibility with the internal market of aid to promote the execution of an IPCEI on the basis of Article 107(3)(b) TFEU, the IPCEI Communication (point 25) requires the Commission to take into account a number of criteria, as elaborated below. Moreover, it requires also that the Commission carries out a balancing test to assess whether the expected positive effects outweigh the possible negative effects (point 26).

(314) Furthermore, the IPCEI Communication (point 27) provides that in view of the nature of the project, the Commission may consider that the presence of a market failure or other important systemic failures, as well as the contribution to a common European interest, is presumed where the project fulfils the eligibility criteria.

(315) Having regard to the conclusion that the general eligibility criteria are fulfilled by the IPCEI Microelectronics, as stated in section 3.3.2 above, and the nature of the IPCEI Microelectronics, the Commission considers that the presence of a market failure or important systemic failure, and the contribution to a common European interest can be presumed in this case.

(316) The analysis of the compatibility criteria, as discussed below, has been performed by the Commission at the level of individual aid beneficiaries[40].

[40] In the Compatibility section 3.3.3, for each aid beneficiary (company) the following is to be understood. Here the "individual project" (not to be confused with the individual components of IPCEI as defined in point 13 of the IPCEI Communication) or the "company's project" is used to refer to the works/activities to be undertaken by a company within the framework of IPCEI Microelectronics, considered at the company's level in their totality. Such individual project is composed of an "R&D&I (part of the individual) project" and an "FID (part of the individual) project". The R&D&I (part of the

3.3.3.1. Necessity and proportionality of aid

(a) Necessity of the aid

(317) According to point 28 of the IPCEI Communication, the aid must not subsidise the costs of a project that an undertaking would anyhow incur and must not compensate for the normal business risk of an economic activity. Without the aid the project's realisation should be impossible, or it should be realised in a smaller size or scope or in a different manner that would significantly restrict its expected benefits. Footnote 24 thereto requires that the aid application must precede the starts of the works, which is either the start of construction works on the investment or the first firm commitment to order equipment or other commitment that makes the investment irreversible, whichever is the first in time. According to point 29 of the IPCEI Communication, the Member State should provide the Commission with adequate information concerning the aided project as well as a comprehensive description of the counterfactual scenario which corresponds to the situation where no aid is awarded by any Member State.

(318) The Commission has verified that all companies have submitted their aid applications to the Member States before the start of their work on their individual projects included in the IPCEI Microelectronics project, therefore the formal incentive criterion, as required by the IPCEI Communication (footnote 24) is met.

(319) The Member States have submitted information demonstrating that the aid has an incentive effect for all aid beneficiaries, i.e. that the aid will induce a change of the behaviour of the beneficiaries by means of allowing them to engage in their IPCEI-covered individual projects in their full ambitious scope and in the time span of the project as notified. More specifically, this information is revealed in the counterfactual scenarios for the aid beneficiaries. For many of the aid beneficiaries it is explicitly stated the information on the counterfactuals is provided for the purposes of the notification only, as no such counterfactual scenario was considered in the company's internal decision making process.

(320) In their majority, these counterfactuals affirm that absent the IPCEI Microelectronics public financing, some of the aid beneficiaries would not undertake their individual projects at all, and others would not undertake their projects as ambitiously and/or as fastly. The aid beneficiaries would instead either limit the size and scope of their individual projects (by limiting their R&D&I activities, or technological ambitions, or FID activities, therefore undertaking much more conservative programmes with reduced levels of ambitions and risks), and (as additional consequence) / or (as a stand-alone consequence) would delay the execution of such (reduced) project by different time[41]. The Member States associate such reduced activities to be alternatively undertaken or the delay in their execution with different negative consequences,

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individual) project contains different R&D&I activities (works). The FID (part of the individual) project contains R&D&I activities (content) and FID activities (content).

[41] In addition to these, for some companies there are also some considerations stated about considering local changes in the company's sites of executions of their projects and of the production that will follow, with impact on the local jobs, etc.

such as promising technologies and processes not being further developed and companies eventually resorting to out-dated and mature technologies, absence or delaying the introduction of the new products to downstream customers, negative impact on upstream and downstream markets, negative impacts on the R&D&I and technical competence, loss of competitiveness, etc.

(321) These counterfactual scenarios are explained by the different types of especially high risks which the Member States associate with the IPCEI Microelectronics and therefrom with the individual projects (such as technological, financial, coordination, dissemination, market, etc.), which would have prevented the companies from undertaking the same projects absent the aid.

(322) The Member States also submit that some of the aid beneficiaries have brought forward certain deliberations of relocation of their activities outside the EU due to, for example, some offers they allegedly received from third countries or due to lower operational costs in those third countries locations, where they already operate certain production facilities.

(323) In all instances where a counterfactual scenario was described in any way (see recitals (320) to (322) above), it was not demonstrated by the Member States by the appropriate evidence that said companies have clearly considered such possibilities as precisely defined and sufficiently predictable alternatives in their internal decision making at the time of taking the decision to apply for the public support. Moreover, it was not further substantiated by any financial calculations of the costs, revenues and profitability of such alternatives to be compared with the scenarios of the aided project.

(324) From the foregoing (recitals (319) to (323) above), the Commission concludes for the purposes of the application of the IPCEI Communication, requiring in point 29 that the counterfactual scenario to be considered should represent "a clearly defined and sufficiently predictable alternative project considered by the beneficiary in its internal decision making", that for all aid beneficiaries there is no counterfactual scenario – i.e. the counterfactuals consist in the absence of alternative projects.

(325) In the absence of clearly defined and sufficiently predictable alternative projects, considered by the beneficiaries, the Commission further verified that the aid was necessary to induce the change of the behaviour of the aid beneficiaries by bringing their individual IPCEI-related projects to a sufficient degree of profitability, corresponding to the company's weighted average cost of capital ("WACC"), as commonly applied by them as minimum internal benchmark for selection of projects. As represented by the funding gap analyses, submitted by the Member States for all aid beneficiaries, the aid is needed in order to cover the funding gap of the individual projects (the net present value of all these projects, calculated by using the respective WACCs as a discounting factor, is negative).

(326) The Member States also submit (also where the aid would not cover the full funding gap (see recital (250) above) that the aid helps to induce the change of the behaviour of the aided companies due to further strategic long-term considerations (such as to offer innovative and differentiating products, to preserve the EU-based technological, research and technical capabilities, strategic KETs importance, strategic security considerations, etc.).

(327) In view of recitals (325) and (326) above, the Commission considers that the Member States have sufficiently demonstrated that the aid measures do not subsidize the costs of the projects that the undertakings would anyhow incur and do not compensate for the normal business risks of the companies.

(328) Considering the fact that the aid measures enable the companies to pursue ambitious projects which would not have been pursued in the absence of IPCEI Microelectronics aid measures, the Commission concludes therefore that the notified aid measures are necessary to induce the change of the behaviour of the beneficiaries.

(b) Proportionality of the aid

(329) According to point 30 of the IPCEI Communication, in the absence of an alternative project, the Commission will verify that the aid amount does not exceed the minimum necessary for the aided project to be sufficiently profitable, e.g. by making it possible to achieve an internal rate of return (IRR) corresponding to the sector or firm specific benchmark or hurdle rate. According to point 31 of the IPCEI Communication, the maximum aid level should be determined with regard to the identified funding gap and to the eligible costs. The aid could reach up to 100% of the eligible costs, provided that the aid amount does not exceed the funding gap.

(330) The Member States have submitted, for all beneficiaries of aid, detailed calculations of the eligible costs for their IPCEI specific R&D&I and FID projects and funding gap calculations. In the individual project descriptions, the contents of the companies' individual R&D&I and FID projects falling into the scope of IPCEI Microelectronics are detailed. In particular, the R&D&I works to be performed, technology risks and challenges, the state-of-the art in the sector concerned are detailed and it is explained how their R&D&I activities bring about important added value in going beyond the state of the art, are of major innovative nature, how the FID allows for the development of *[…]* high research and innovation content and/or fundamentally innovative *[…]* processes and contains a very important R&D&I component. They also detail the eligible costs for the R&D&I and FID projects.

(331) In its assessment of the eligibility of the costs, for the individual R&D&I projects, the Commission has, firstly, verified individually for all aid beneficiaries, that their projects contain R&D&I of major innovative nature, going beyond the state-of-the art in the sector concerned[42]. This verification was based on the R&D&I works to be performed, the technology challenges and technology risks to be overcome, as demonstrated by each company, and checked item by item and technology by technology.

(332) In particular, having regard to the specificities of the microelectronics sector and the companies' individual R&D&I projects contained in this IPCEI, for the purpose of assessing the innovative character of the R&D&I undertaken by the companies participating in the IPCEI, the following approach was taken.

[42] On this point, the requirements of the IPCEI Communication are more ambitious than in the R&D&I State aid framework.

(a) The body of technical and scientific open literature was verified for all the specific technologies addressed within the IPCEI. It included scientific and technical journals and conference proceedings and wherever needed the patent literature was also checked. All technologies for which the known technology barriers are high (e.g. heterogeneous integration of materials in semiconductor technology, individual pixel addressing in some specific imager technologies, high frequency components, extreme ultraviolet technology) were double-checked with the most advanced scientific and technology literature.

(b) From the output point of view, when the category of an intended product has a very wide spectrum of applications (e.g. pressure or motion sensors, photonic or digital components), it was verified that the innovations brought by the IPCEI are not merely incremental but are such to overcome a major limitation making it impossible or slowing down strongly their introduction due to the associated risks (e.g. when it comes to technology integration of several complex technologies).

(c) The complexity of the technologies and of their integration was assessed against the scientific and technical information. It was also consistently verified for all technologies that the targeted advance in functionality is substantial and necessitating high innovation to be reached, and not merely an incremental evolution of the technologies existing and embedded in products on the market.

(333) Based on the analysis for each beneficiary, performed as described in the preceding recitals, the Commission therefore concludes that the individual R&D&I projects of all aid beneficiaries contain R&D&I of major innovative nature, going beyond the state-of-the art in the sector concerned.

(334) Secondly, the Member States have verified and confirmed that the related R&D&I costs of each aid beneficiary comply with the Annex on eligible costs to the IPCEI Communication. The Commission has checked these costs and considers that they fulfill the conditions set out in the Annex to the IPCEI Communication.

(335) For the individual FID projects, the Commission has verified individually for all aid beneficiaries, in order to determine whether it qualifies as FID under the IPCEI Communication, that the industrial deployment concerns "the development of a new product or service with high research and innovation content and/or the deployment of a fundamentally innovative production process[43]" and does not constitute "Regular upgrades without an innovative dimension of existing facilities and the development of newer versions of existing products[44]", "the upscaling of pilot facilities, or [to] the first-in-kind equipment and facilities which cover the steps subsequent to the pilot line including the testing phase, but neither mass production nor commercial activities[45]", and "follows on from an R&D&I activity and itself contains a very

[43] Point 22 of the IPCEI Communication, first sentence.

[44] Point 22 of the IPCEI Communication, second sentence.

[45] Footnote (1) in the Annex to the IPCEI Communication.

important R&D&I component which constitutes an integral and necessary element for the successful implementation of the project[46]". In relation to the costs, the Commission has assessed, in particular, that they relate to "the capital and operating expenditures (CAPEX and OPEX), as long as the industrial deployment follows on from an R&D&I activity and itself contains a very important R&D&I component[47] which constitutes an integral and necessary element for the successful implementation of the project[48]".

(336) Having regard to the specificities of the microelectronics sector concerned and the companies' individual FID projects contained in this IPCEI, the Commission has assessed the eligibility of FID costs for each aid beneficiary according to the criteria in recital (335) above, in the following manner.

(337) The Commission has verified and finds for all aid beneficiaries, for each FID project, that it concerns either a new product with high research and innovation content or a fundamentally innovative production process.

(338) The Commission has verified and finds for all aid beneficiaries, for each FID project, that the industrial deployment concerns technologies with high R&D&I content or fundamentally innovative nature, and these highly innovative technologies are a result from a preceding R&D&I activity but yet they still require very important R&D&I to be carried out even after the R&D&I phase, i.e. to put these technologies into FID requires very important R&D&I; as such, the FID of these specific technologies contains a very important R&D&I component on its own, and this R&D&I in the FID phase is indispensable for the successful FID of the technologies.

(339) In relation to the very important R&D&I component, the Commission has verified and finds that for all beneficiaries an adequate demonstration of the very important (in quantitative and/or qualitative terms) R&D&I activities in their FID which constitutes an integral and necessary element for the successful implementation of the individual project, is provided. In particular, the Commission verified for each FID project that the planned important R&D&I during the FID, necessary to solve outstanding technological roadblocks, among others in terms of process integration, design stability, testing, packaging of components and/or security and safety of components, in the context of the complex technologies and large number of processes involved, is demonstrated. Mere engineering work accompanying normal activities of first industrial deployment does not constitute the required R&D&I in FID. In particular, the assessment of the very important R&D&I component in the FID of each beneficiary took into account the issues as specified in recitals (340) to (343) below.

(340) The assessment took into account, for each FID project specifically, the integration of processes in the industrial environment, the necessity of process,

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[46] Point (g) in the Annex to the IPCEI Communication.

[47] The wording of the IPCEI Communication implies that the very important R&D&I component that needs to be embedded in the FID costs in order for these to be eligible constitutes a limit both in scope and time ("as long as") on the eligible FID costs.

[48] Point (g) in the Annex to the IPCEI Communication.

equipment and/or component redesign in relation with the complexity of the line, the technological complexity and progress beyond the state-of-the-art of the targeted components and systems, the applications addressed and their specific constraints in particular in terms of safety and security in relation to the components it embarks. When assessing the setting up of processes, activities are only considered eligible where they relate to the introduction of processes that transfer the R&D&I performed before FID and are critical for the functionality of the resulting product. These activities were assessed against the most up-to-date publicly available information on semiconductor manufacturing (including scientific and technical literature journals, corporate technical scientific publications, corporate and news, patents).

(341) In its assessment, the Commission has verified that the industrial deployment is not a mere regular upgrade, without an innovative dimension, of existing facilities, or a development of newer versions of existing products or technologies.

(342) In its assessment, the Commission has considered that where FID costs and the embedded R&D&I do not relate to the highly/fundamentally innovative technologies the beneficiary is developing, these are not eligible. Where the R&D&I in FID does not take place before the end of FID (end date in line with the IPCEI Communication), the FID costs are not eligible.

(343) The Commission has verified that, where a beneficiary is upscaling from a pilot line to a full scale line, the R&D&I embedded in the FID of the technology that it will be performing with the production line is very important. Where a beneficiary is building a new line (without upscaling from a pilot line), the Commission has verified it is not merely duplicating an existing line but that it is a new line for the FID of the highly innovative technology (in order to be able to put the highly innovative technology into FID), and that the very important R&D&I embedded in the FID of the technology that it will be performing with the line is demonstrated. Where a beneficiary is upgrading or extending an existing line with new tools, the Commission has verified that it is demonstrated for these tools that they are integrated into the line for FID of the highly innovative technology. The demonstration of R&D&I to connect the tools with the purpose of making them work together at higher productivity and yield required by mass production is not sufficient to make the purchase of the tool an eligible cost.

(344) The Commission has also verified that FID does not cover mass production or commercial activities. Also in relation to this criterion (see footnote 47 above) the Commission has verified the end date of the FID for each beneficiary, so that to ensure that only costs incurred before this end date are considered eligible. To this end, the Commission took into account the specificities of the microelectronics sector as explained by the Member States, for example the fact that the Member States affirm that during FID some first produced test parts could be transferred to dedicated downstream partners for assessing either the new technology or the new products, while important R&D&I in FID still needs to be performed. Therefore for each beneficiary the Commission considered both the presence of the very important R&D&I component in FID (as detailed in recitals (339) to (343) above) and the volume of outputs of the FID process. To analyse the latter, the Commission has considered that FID costs are not

eligible anymore from the moment the volumes of outcoming products and/or sales during alleged FID could point towards mass production or commercial activities, as opposed to testing as described above. As a result, the Commission assessment confirms that the notified durations of the FID phase for the purposes of application of the IPCEI Communication of all aid beneficiaries comply with the requirement not to cover mass production or commercial activities.

(345) With regard to the eligible FID costs, the Commission has also verified, for cost items that are depreciated during several years, that only depreciation costs until the end of FID are included in the eligible costs[49].

(346) With regard to the operating costs which should be limited both in scope and in time to the R&D&I that the FID entails, the Member States have verified and confirmed that this requirement is complied with. The Commission has checked these costs and considers the requirement fulfilled.

(347) The Member States have verified and confirmed that the FID costs comply with the Annex to the IPCEI Communication. The Commission has checked the FID costs and considers that they fulfill the conditions set out in the Annex to the IPCEI Communication.

(348) Based on the above, the Commission finds that the costs notified by the Member States in relation to all aid beneficiaries fulfil the requirements of the Annex to the IPCEI Communication.

(349) The Commission reviewed in detail the funding gap calculations provided by the beneficiaries and verified the main assumptions in those calculations against publicly available data.

(350) Taking into account the foregoing, the Commission considers that the aid to all beneficiaries does not exceed the individually identified funding gap of each beneficiary and does not exceed the eligible costs.

(351) Therefore the Commission considers that the aid to be granted by the notifying Member States is proportionate.

3.3.3.2. Prevention of undue distortions of competition and balancing test

(352) According to point 40 of the IPCEI Communication, the Member State should provide evidence that the proposed aid measure constitutes the appropriate policy instrument to address the objective of the project.

(353) The Member States submit in their notifications of the measures their reasoning as to why State aid is the appropriate policy instrument to support the IPCEI Microelectronics. In their view, due to the exceptional size of the project and the synergies it requires from the various partners, the IPCEI Microelectronics could

[49] While verifying the funding gap calculations, for buildings or equipment used for the IPCEI project, which still have a value at the end of the project, the Commission has verified that this terminal/residual value is added to the revenues in the last year of project's financial projection to determine the project's specific funding gap.

not be achieved and such technological breakthroughs could not be created without the support of the Member States involved in the financing of this project; otherwise the participating companies would have focused on their own roadmaps to the detriment of innovations whose spillover effects will largely benefit EU ecosystems.

(354) The French authorities further submit additional considerations as to why other policy instruments would be inappropriate alternatives to State Aid. The French authorities consider that the use of regulation to implement the IPCEI Microelectronics has little practical consistency; that an increase of funding of public research would not be appropriate, as even though R&D activities must be carried out simultaneously in public laboratories and in companies, it is the latter which have the essential role to ensure the development of new technologies and their first industrial deployment, as companies are the best placed to demonstrate the viability of the innovation. Income tax credits based on R&D expenditures provide no incentive for the deployment of the IPCEI Microelectronics.

(355) The Commission shares the views of the Member States that given the level of ambitions pursued by IPCEI Microelectronics, its size and numerous collaborative interactions that it will induce, the public support through the notified State aid measures is the appropriate policy instrument to address the IPCEI Microelectronics' objectives.

(356) According to point 41 of the IPCEI Communication, aid can be declared compatible if the negative effects of the aid in terms of distortions of competition and impact on trade between Member States are limited and outweighed by the positive effects in terms of contribution to the objective of the common European interest. The assessment of the potential negative effects of the aid under the IPCEI Communication needs to consider, in particular, the effects on competition between undertakings in the product markets concerned, as well as risks of market foreclosure and dominance (points 42 and 43 of the IPCEI Communication).

(357) The Commission's analysis of undue distortions to competition is always specific to the particular case. The IPCEI at hand involves an unusually large number of companies, each with several products present in various product markets. Key Enabling Technologies by nature diffuse to several applications along the value chain, which further increases the number of markets potentially affected by the State aid measures. For this reason, in this particular case, the Commission adopted a two step approach, as described below, in order to identify potential significant competition distortions which might result from the aid measures.

(358) First, the Commission filtered, based on uniformly available metrics, the companies for which the risk of competition distortions may be considered more likely. Second, for the group of companies where the first step resulted in the conclusion that the competition distortions could be more likely, a more detailed assessment of market conditions and competitive forces has been carried out to assess the risk of competition distortions.

(359) As for the first step (filtering companies), the Commission obtained data from the Member States on the aid beneficiaries' past production values by 8-digit

PRODCOM classification of products categories they intend to produce as a result of the aided project.[50] Two main indicators have been used for this assessment:

a) Indicator 1: The share of the company's production value in EU production in the PRODCOM category over the last three years with data available. The reason behind this indicator is that aid flowing to companies with larger sectoral production shares is likely to be more distortive to competition because those beneficiaries may use the aid to expand an already significant production share.

b) Indicator 2: The ratio of aid on annual production value. This indicator is an approximation for the ability of the aid to increase the production share of the recipient at the cost of competitors.

(360) Taken together, the two indicators filter the companies that have been showing high productions shares in the EU in the aided products and receive an amount of aid that is likely to expand their production share further. Higher values on these two indicators may also imply a higher potential risk of market foreclosure and dominance.[51]

(361) Considering production shares and aid amounts (relative to the production values), the Commission identified a list of companies for which the aid may potentially raise more significant competition concerns.

(362) In a second step, the Commission assessed the detailed information about the competitive landscape these companies face, as provided by the Member States, including the risk of market foreclosure and dominance.

(363) In addition, in order to counter these potentially higher competition concerns, including the risk of market foreclosure amd dominance, raised for the specific companies, the Commission has verified that it has been notified that each of these companies individually undertook to engage in significant additional actions for the dissemination of the specific knowledge and results generated by these companies in relation to the IPCEI Microelectronics and on their specific FID carried out, beyond their business-as-usual, for the benefit beyond their existing ecosystems, and beyond the participating Member States.

(364) Member States have notified substantial additional spillovers to be effected by all identified companies. Thus, on dissemination of IPR-protected IPCEI Microelectronics results, each of these companies will license to certain types of companies and research organisations and under certain terms, which has been

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[50] According to the PRODCOM statistics on the production of manufactured goods. PRODCOM sectoral data has been used in State aid control for example in the ETS Guidelines and the Environmental and Energy Aid Guidelines.

[51] Due to the scope of this case, involving several beneficiaries each active in multiple geographic and product markets, the Commission did not define relevant markets as in its previous State aid case practice. Doing so would not have been practical in the case. The indicators used by the Commission to filter companies as raising potential competition concerns could be nevertheless considered as proxy to horizontal market shares. For example, a larger share in EU production value might be possibly correlated with a larger market share in related relevant markets. These indicators therefore approximate the likelihood that the aid strengthens a horizontal bottleneck position of the beneficiary in a market. The presence of such horizontal bottlenecks also makes upstream and/or downstream foreclosure more likely.

considered by the Commission as sufficiently addressing the potential concerns of distortion of competition.

(365) On FID-spillovers (and also, to a certain extent, on non-IPR-protected knowledge) which has been considered by the Commission as a vital way to ensure that the benefits of the IPCEI Microelectronics will be made widely available to the industry and research/ scientific community beyond the participating companies and Member States, and thus actively counterbalancing the possible competition distortion concerns, the Member States have notified that each of these companies will undertake substantial additional actions, going beyond its business as usual, and under certain terms, in order to spillover the benefit from its FID. A non-exhaustive illustrative summary of these extra IPCEI Microelectronics-induced spillovers includes:

- To carry out[52] MPW (multi-project wafer) runs on the respective company's production lines, specified by each company by their number per year, by years for which to be provided, and by conditions for the provision (which in general refer to fair market prices), to the benefit of companies in any Member State (regardless of its participation in IPCEI Microelectronics), or to increase significantly such MPW runs compared to the company's usual business;
- To provide for free the company's specific input for such MPW (for example *[...]*);
- To set up a new company together with external partners *[...]*, especially for SMEs and Start-ups;
- To set up a *[...]*, where to provide access to the company's *[...]*;
- To provide access to the company's *[...]* to SMEs and ROs;
- To enable universities, ROs and SMEs to generate *[...]*;
- To support *[...]* based on the *[...]* technology and learnings from the IPCEI Microelectronics activities;
- To provide the new technologies and components to;
- *[...]*;
- To set up within the IPCEI Microelectronics a *[...]* support programme to support *[...]* in investment and RDI generation, which will be open also to new suppliers;
- To hold *[...]* events with established and not-yet identified suppliers; etc.

For the above listed actions, the companies undertook to follow a proactive approach and to ensure certain numerical targets are reached.

(366) In addition, additional dissemination activities will be performed by these companies, such as the organisation of hackathons, workshops, drafting textbooks on the specific technology, internship programs, tutoring of SMEs, etc., which will be targeting specialized technical audience and therefore enabling it to uptake the technical knowledge and experience generated due to the IPCEI Microelectronics.

(367) Based on the careful assessment of these additional actions, the Commission considers that they are adequate to counter the potential higher competition

[52] This is relevant for companies that are foundries, IDMs and vertically integrated companies.

concerns posed for certain companies and also contribute to the positive effects of the IPCEI Microelectronics.

(368) The overall positive effects of the IPCEI Microelectronics encompass its concrete contribution to several objectives of common European interest (as specified in recitals (281) to (290) above) and its benefits of wider relevance to the EU economy, as ensured by the combination of the spillovers at the level of the IPCEI Microelectronics with the ones at individual companies' level (see recitals (293) to (299) above), including the additional actions as specified in recitals (364) to (367) above.

(369) The Commission considers therefore that the possible negative effects of the IPCEI Microelectronics in terms of potential distortions of competition are limited and outweighed by the overall positive effects of the IPCEI Microelectronics.

3.3.3.3. Transparency

(370) The transparency requirement, specified in section 4.3 of the IPCEI Communication, is fulfilled (see recital (258) above).

3.3.4. Reporting obligation

(371) According to point 49 of the IPCEI Communication the execution of the project must be subject to regular reporting.

(372) As notified by the Member States, the annual execution of the IPCEI Microelectronics activities as regards the technical advancements and individually committed spillovers, will be subject to reporting by the participating companies (to their national funding authorities), to annual reports on the progress and results of each of the technology fields and to annual report on the progress of the IPCEI Microelectronics as a whole (including through key performance indicators), as described in recitals (92), (93) and (98) above.

(373) The Member States must provide the Commission with an annual report, containing the progress and results of the IPCEI Microelectronics, the technology fields and the companies. These reports will include detailed reporting on the actions undertaken (e.g. number of SMEs pro-actively approached in which Member States) and results achieved by the companies in relation to the spillover actions which the companies have committed themselves to. The Member States have confirmed they will provide this reporting.

(374) The Commission therefore considers that the reporting obligation on the execution of the IPCEI Microelectronics should be fulfilled as described above.

3.3.5. Conclusion on compatibility

(375) Based on the assessment under the IPCEI Communication, the Commission concludes that the notified aid measures are compatible with Article 107(3)(b) TFEU.

3.4. Additional observations

(376) Since the United Kingdom notified on 29 March 2017 its intention to leave the Union, pursuant to Article 50 of the Treaty on European Union, the Treaties will cease to apply to the United Kingdom from the date of entry into force of the withdrawal agreement or, failing that, two years after the notification, unless the European Council, in agreement with the United Kingdom, decides to extend that period. As a consequence, and without prejudice to any provision of the withdrawal agreement, this decision only applies to the UK until the United Kingdom ceases to be a Member State.

4. CONCLUSION

(377) In view of the above and in light of notifications of the Member States, the Commission has decided:

- not to raise objections to the aid on the grounds that it is compatible with the internal market pursuant to Article 107(3)(b) of the Treaty on the Functioning of the European Union.

If this letter contains confidential information which should not be disclosed to third parties, please inform the Commission within fifteen working days of the date of receipt. If the Commission does not receive a reasoned request by that deadline, you will be deemed to agree to the disclosure to third parties and to the publication of the full text of the letter in the authentic language on the Internet site: http://ec.europa.eu/competition/elojade/isef/index.cfm.

Your request should be sent electronically to the following address:

European Commission,
Directorate-General Competition
State Aid Greffe
B-1049 Brussels
Stateaidgreffe@ec.europa.eu

Yours faithfully
For the Commission

Margrethe VESTAGER
Member of the Commission

Annex – Glossary of acronyms

5G	5th generation of wireless communication technology
ADAS	Advanced Driver-Assistance Systems
[…]	*[…]*
AMR	Anisotropic MagnetoResistance
AMCME	Advanced Methods for Chip Manufacturing Enhancement
APD	Avalanche Photodiode
AR	Augmented Reality
AR/VR	Augmented Reality / Virtual Reality
ASIC	Application Specific Integrated Circuit
[…]	*[…]*
BCD	Bipolar CMOS DMOS
BEOL	Back-End of Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
C&F	Concept and Feasibility
CAD	Computer Aided Design
CD	Critical Dimension
CIS	CMOS Image Sensor
CMOS	Complementary Metal Oxide Semiconductor
CS	Compound Semiconductor
DC	Direct Current
DMOS	Double-diffused Metal Oxide Semiconductor
DUV	Deep UltraViolet
[…]	*[…]*
E^2PROM	Electrically Erasable Programmable Read-Only Memory
eFPGA	embedded Field Programmable Gate Array
eNVM	embedded Non Volatile Memory
EUV	Extreme Ultra Violet
eWLB	embedded Wafer Level Ball Grid Array
FDSOI	Fully Depleted Silicon On Insulator
FEOL	Front-End of Line
[…]	*[…]*
FinFET	Fin Field Effect Transistor
FPA	Focal Plane Array
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
[…]	*[…]*
[…]	*[…]*
HV	High Voltage
IC	Integrated Circuit
ICT	Information and Communication Technologies
IDM	Integrated Device Manufacturer
[…]	*[…]*
III-V	Compound semiconductor materials for the columns III and V of the Mendeleiev periodic table

InGaN	Indium Gallium Nitride
InP	Indium Phosphide
IoT	Internet of Things
IP	Semiconductor intellectual property core
IPCEI	Important Project of Common European Interest
IR	InfraRed
IYM	Internal Yield Management
KET	Key Enabling Technology
LED	Light Emitting Diode
LIDAR	Light Detection And Ranging
[…]	*[…]*
LWIR	Long Wavelength InfraRed
MCU	MicroController Unit
MEMS	MicroElectroMechanical System
mmWave	Millimeter wave
MPW	Multi-Project Wafer
MRAM	Magnetic Random Access Memory
MOCVD	Metal Organic Chemical Vapor Deposition
NA	Numerical Aperture
NVM	Non-Volatile Memory
OEM	Original Equipment Manufacturer
OxRAM	HfO2-based oxide-based Random Access Memory
P&R Software	Place and route software
PA	Power Amplifier
PCM	Phase Change Memory
PCRAM	Phase Change Random Access Memory
PDK	Process Design Kit
PIN	Positive Intrinsic Negative
[…]	*[…]*
RF	Radio Frequency
RF-SOI	Radio Frequency - Silicon On Insulator
RGB	Red Green Blue
RO	Research Organisation
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiPM	Si PhotoMultiplier
[…]	*[…]*
SME	Small and Medium Enterprise
SoC	System on Chip
SOI	Silicon On Insulator
SPAD	Single Photon Avalanche Diode
SRAM	Static Random Access Memory
TIA	Transimpedance Amplifier
TSV	Through Silicon Via
TV	Television

[…]	*[…]*
UV	UltraViolet
[…]	*[…]*
WP	Work Programme or Work Package