

-NANOSIL NoE - ICT/FP7 - *EU-Russia meeting, October 2008*

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Title: Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications

www.nanosil-noe.eu

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-NANOSIL NoE-FP7 -



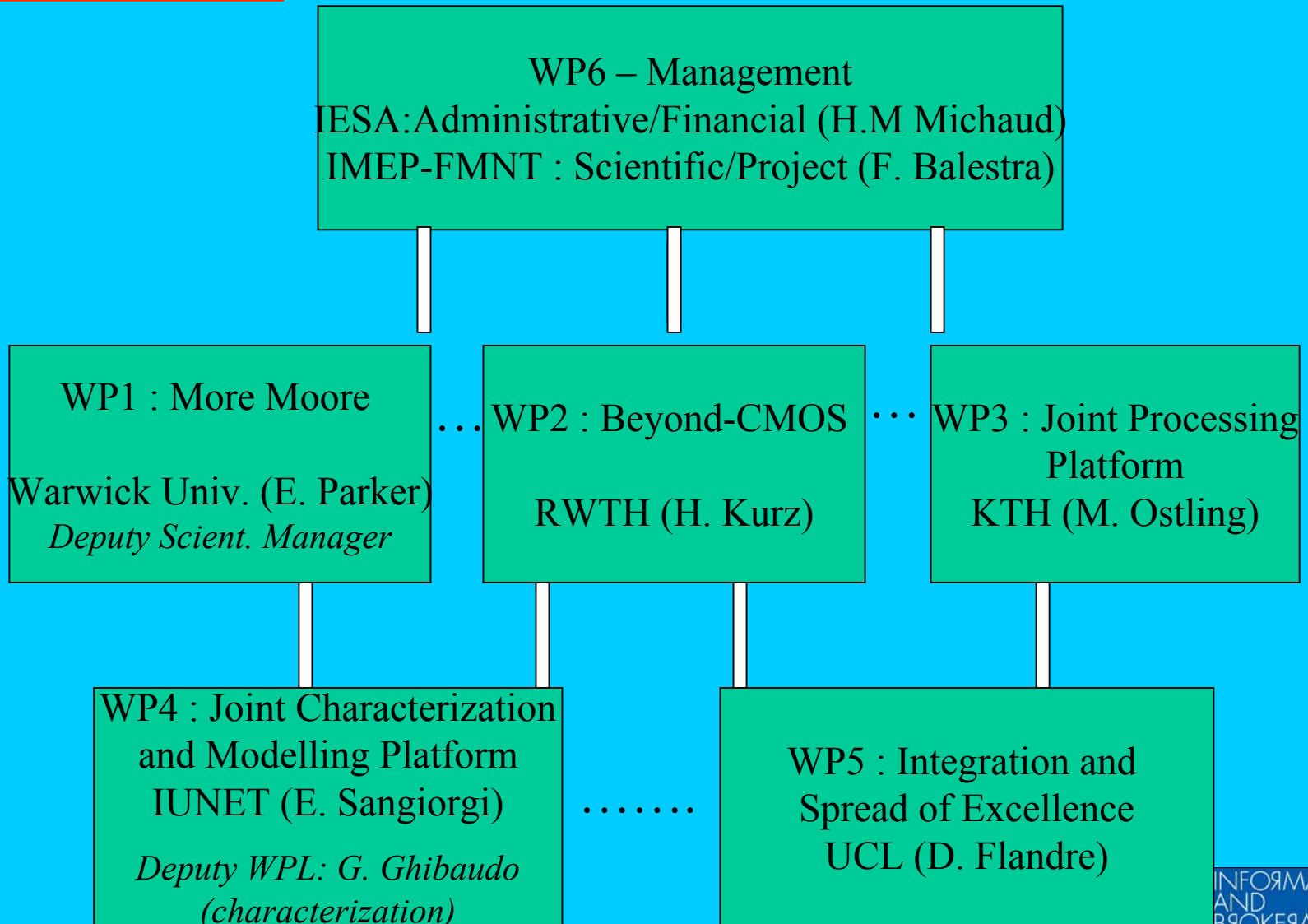
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NANOSIL objectives

- ⇒ 29 Partners from 11 European countries:
main European Labs, Research Centres in this field
- ⇒ Push the limits of Si integration down to nanometric dimension
- ⇒ Work on N+4 technology node and beyond using flexible platforms
- ⇒ Overcome the number of research challenges of ultimate CMOS and beyond-CMOS nanodevices in order to speed up technological innovation for the Nanoelectronics of the next 2-3 decades
 - ⇒ Will allow **integration** of Si-based innovative CMOS and emerging non-CMOS devices on one Si chip, which is a strategic issue for the next IC generations
- ⇒ Prepare the path for future industrial applications in the field of communications, computing, consumer electronics, health, environment, etc.

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NANOSIL WPs



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NANOSIL projects

- *More Moore:*

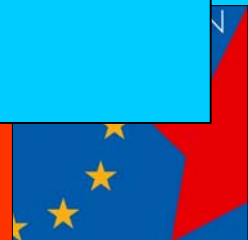
- FP1.1: Appraisal of **new channel materials** for end of CMOS era
=> sSOI, sSiGeOI and sGeOI, various channel orientations, etc.
- FP1.2: Routes to realisation of **very low Schottky barrier** contacts for end of CMOS era
=> cover a wide spectrum of silicide materials and dopants for the realization of dopant-segregated metallic junction ; integration of such junctions on strained and unstrained layers on insulator
- FP1.3: Identification and appraisal of **novel gate stack materials/combinations** for end of CMOS era
=> $k \cdot \Delta E > 70$

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NANOSIL projects (2)

- *Beyond CMOS:*

- * FP2.1: Evaluation of the prospects of **1D nanowires** for the post-CMOS era
=> with strain, low Schottky barrier contacts, high k/metal gate stacks, parallel nanowires
- * FP/AS2.2: Investigation of the prospects for **carbon structures - especially graphene**, and their technological potential
- * FP2.3: Assessment of the performance of **new nanoelectronic switches**:
=> *impact ionisation (IMOS), tunnelling devices (TFET, RTD), NEM-FET* in order to determine if they can form the basis of new MOS device functionality with very low subthreshold slopes
- * FP2.4: Investigation of routes for producing high densities ($> 10^{12}\text{cm}^{-2}$) of **nanodevices (nanodots, nanowires) by templated self-assembly**, and assessment of their technological potential



NANOSIL projects (3)

- ***Visionary projects:***

=> *discussion Forums, brainstorming activities and Workshops* in More Moore (WP1) and Beyond-CMOS (WP2) areas to **generate new ideas** and identify the **most promising topics** for future information technology

- ***Joint Processing Platform:***

- * *Execute* batch processing for the flagship projects

- * *Coordinate* processing involving several partners

- * *Fabricate* MOSFETs and test structures for the Joint Characterization and Modelling Platform

- * *Strengthening projects* for the development and integration of new processes especially needed by the flagship projects

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NANOSIL projects (4)

- *Joint Characterization and Modelling Platform*

- * *Integration and validation* of the modelling approaches and tools against ad-hoc, well-characterized template devices
- * *Design* the test structures to be fabricated in the joint processing platform of WP3 for the implementation of characterization experiments aimed at the calibration of the modelling tools.
- * *Bring together* the most promising characterization techniques and modelling tools and methods to tackle the main device physical challenges
- * *Strengthening projects* for the tuning and validation of modelling and characterization techniques to be exploited in the frame of the Flagship Projects

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Impact of NANOSIL on European structuring

- Establish **close links with other European Projects** (IPs, STREPs, etc.) in the same field and ENIAC
 - Strengthen interaction between the **Scientific Community** and the **European Industry**
 - Analyse and develop **links with the National projects** in the same field in order to enhance the overall efficiency of the European research in Nanoelectronics
- => **NANOSIL will act as a cluster of projects**, existing at the beginning or new ones to be proposed, providing they were sufficiently forward-looking
- Consolidate a **durable EU Network** of researchers, based on the **SINANO Institute**, leading to a **Virtual Centre of Excellence** for:
 - studying and validating new concepts, novel materials and technologies, innovative device architectures using joint platforms
 - updating roadmaps
 - speed up technological development

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-SINANO Institute-

Russia-EU meeting, Oct. 2008

Francis Balestra, Director of the SINANO institute

⇒Members:

18 laboratories from 10 European countries, representing the main partners from the Scientific Community involved in the networking activities of the previous FP6 SINANO NoE

⇒ Legal entity: French Association

⇒ Structure:

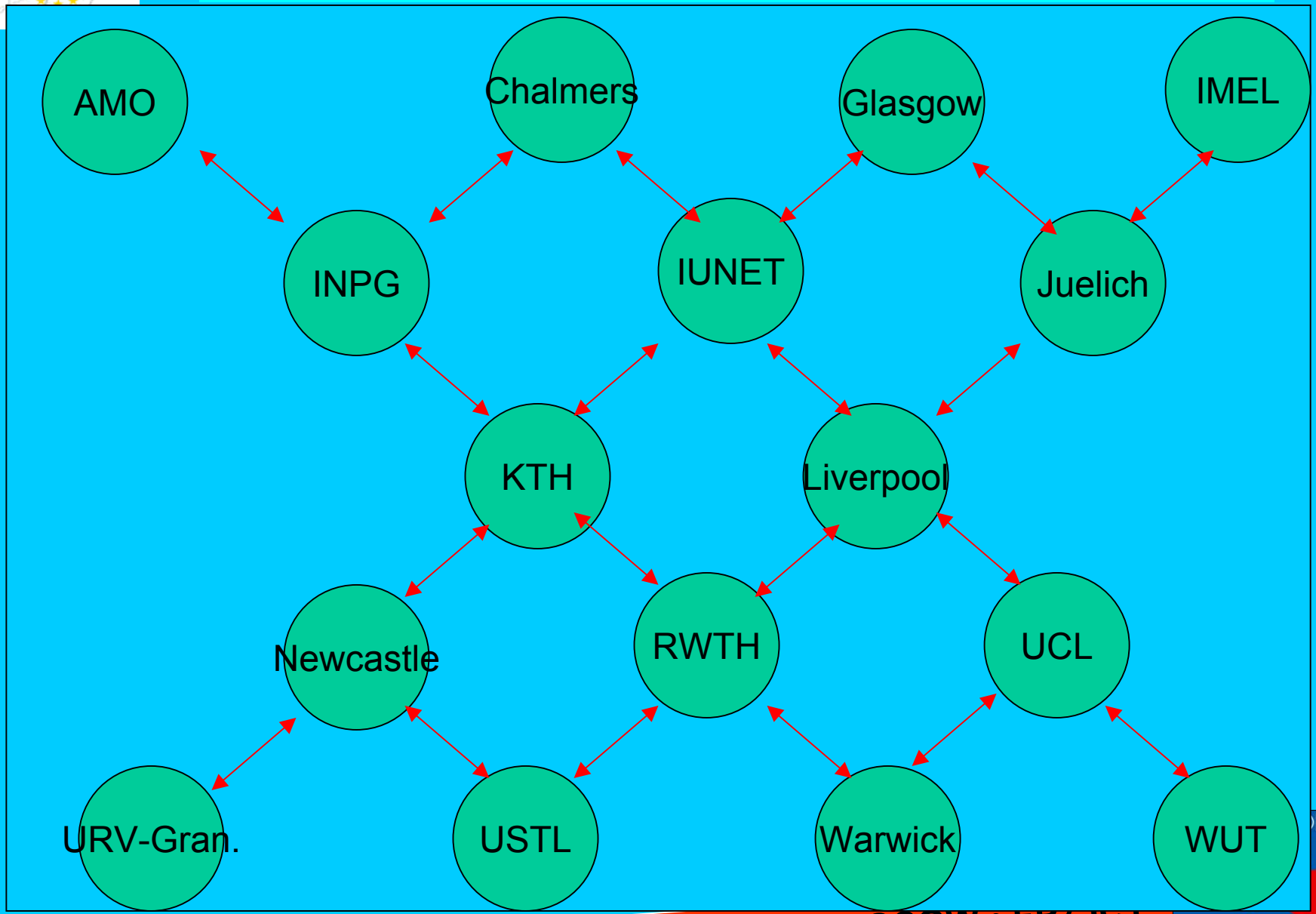
- General Assembly (all the Members)
- Governing Board (5 Members representing all the research areas)
- Director of the Institute

www.sinano.org

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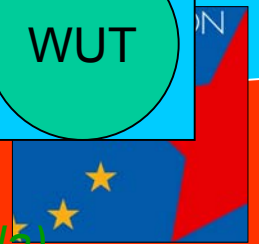


Members of the Sinano Institute



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Francis Barreca => Association opened to other Members (recently: Tyndall, Uppsala)





Main Objectives (1)

- * Establish a **durable EU Network of researchers** from the European Scientific Community in order to form a distributed Centre of Excellence in the Nanoelectronics field
- * Carry out a role of **representation and coordination** of the associated Organizations in this area
- * **Pool and co-ordinate human and physical resources** of the best proven laboratories in the ultimate devices arena, creating a truly multi-disciplinary network
- * Explore the science and technology aspects for **n+4 technology nodes and beyond**
- * Research work for enhancing **device integration, functionality and performance** in order to meet the future demands in electronic components and systems.

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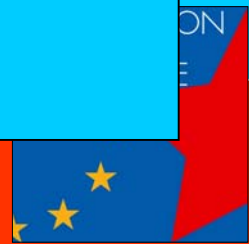




Main Objectives (2)

- * Provide a forward-look and develop collaborations with industry, aimed at the industrial exploitation of innovative ideas and concepts
- * Activities centred on More Moore and Beyond CMOS + links other ENIAC domains (MtM: micro-nanosystems, RF, etc.)
- * Work carried out through joint flexible processing, characterisation and modelling platforms
- * Perform training activities, University curricula, Workshops to develop high competence levels in Europe
- * Participate in roadmap definition
- * Help in the coordination of European, National and Regional activities and promote the participation of the associated Organizations in national and international research projects

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The SINANO Institute

⇒ **About 640 scientific and technical staff** (Professors, Researches, Post-docs, PhDs, Engineers, Technicians) working together in the field of Nanoelectronics in the SINANO Institute

⇒ All the necessary processing, characterization and modelling facilities to tackle:

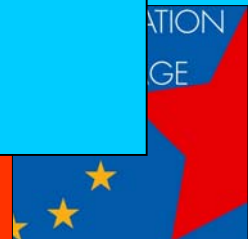
- *the growth of novel materials*
- *ultimate technological processes and nanodevices*
- *the understanding of new physical phenomena*

for the nanoelectronics of the next decades

⇒ About **20** International Conferences and Summer Schools organized by the SINANO members *every year*

⇒ About **140** invited papers in International Conferences/*year*
and **30** books or book chapters/*year*

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Impact of the SINANO Institute

⇒ The SINANO Institute will provide long-term stability on which Europe can rely for studying and validating new concepts, novel materials and nanotechnologies, innovative device architectures in order to speed up technological development

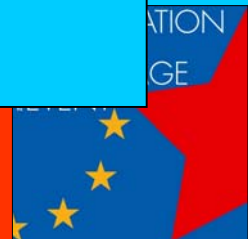
⇒ It will become a fully established and operational structure:

- * by full exploitation of competences and specialization of Partners
- * by consolidating the joint process-charac-modelling platforms
- * by strengthening links to industry

⇒ Become one of the main international scientific partners in this field

⇒ Play an important role in European structuring and programs, and certainly strengthen the overall efficiency of the European research in Nanoelectronics

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Thank you!

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