EECA ESIA

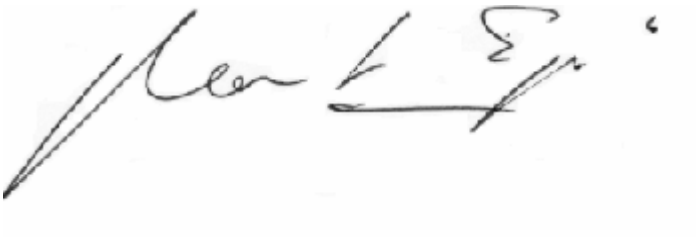
European Semiconductor Industry Association

Ms Marianne Klingbeil
Head Of Unit
Directorate A-2
DG Environment
European Commission
BU-5 05167
B-1049 Brussels

Dear Ms Klingbeil,

Please find enclosed comments, which are submitted by the European Semiconductor Industry Association (EECA-ESIA) as part of the RoHS stakeholder consultation process. The European Semiconductor Industry Association is fully committed to the implementation of and compliance with the RoHS directive and would like to ask for the Commission's continued cooperation to come to a speedy resolution of the issues surrounding the RoHS review process.

Yours sincerely,



Mr Martin Spät
Director EECA-ESIA

The European Semiconductor Industry Association (ESIA), part of the European Electronic Component manufacturers' Association (EECA), represents the European-based manufacturers of semiconductor devices. The semiconductor industry provides the enabling technology, which is at the forefront of the development of the digital economy. The sector supports over 85,000 jobs in a market currently valued at around €28.5 bn. There are around 80 production sites in Western Europe.

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9. Lead in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead content of more than 85% in proportion to the tin-lead content (exemption until 2010)

ESIA supports this request.

Do feasible substitutes currently exist in an industrial and/or commercial scale?

No. There are no known feasible substitutes for the highest pin counts in microprocessors.

Do any restrictions apply to such substitutes?

There are no known substitutes with equal reliability for high pin counts. Also alternatives contain materials with recycling restrictions.

What are the costs and benefits and advantages and disadvantages of such substitutes?

There are no known substitutes with equal reliability for high pin counts.

10. Lead in high melting temperature type solders (i.e. tin-lead solder alloys containing more than 85% lead) and any lower melting temperature solder required to be used with high melting temperature solder to complete a viable electrical connection

ESIA supports this request.

- *Do feasible substitutes currently exist in an industrial and/or commercial scale?*

No

Additional information

One common application using high melting temperature solders is found in the internal solder joints of certain components. During the component manufacturing process, lead solder bumps (>85% lead) are connected to the bond pads (circuitry) of the chip. The high melting point tin-lead alloy has high electrical conductivity and has unique mechanical properties that make the material malleable and better able to withstand both temperature and physical stress. Such properties ensure fewer defects during manufacturing and high reliability throughout the life of the component.

The chip with the high melting point lead solder bumps must then be attached to the organic substrate (organic semiconductor package) as a semiconductor device. The organic substrate, however, cannot withstand elevated temperatures. Therefore, the chip with high melting point lead solder bumps is attached to the substrate circuitry by using a very small amount of lower temperature tin-lead solder alloy. The resulting solder joint is a mixture of the high and lower melting point -lead solders, consisting of approximately 65-80% lead.

A graphic description of the chip, substrate (package) and resulting solder joint is shown below

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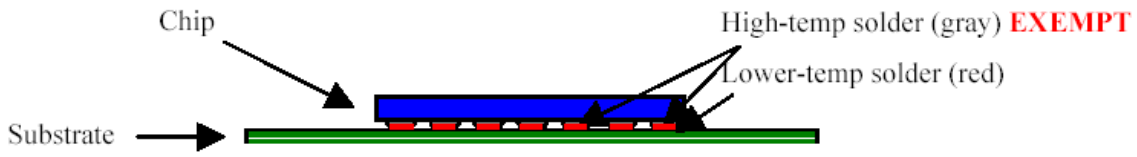

: Viable lead-free solutions are currently not available to attach the chip with high temperature solder bumps to the package substrate. This is due to the technical properties of the lead-free solders, which are stiff and cause stress on the chip circuitry. These stresses cause failures to the circuitry of the chip, creating a non-functioning semiconductor.

- *Do any restrictions apply to such substitutes?*
No substitutes are known; therefore the question cannot be answered meaningfully.

- *What are the costs and benefits and advantages and disadvantages of such substitutes?*
No substitutes are known; therefore the question cannot be answered meaningfully.
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11. Lead in solders to complete a viable electrical connection internal to certain Integrated Circuit Packages (Flip Chips) (exemption until 2010)
Do feasible substitutes currently exist in an industrial and/or commercial scale?

No feasible **lead free** substitutes exist today in an industrial or commercial scale for interconnect bumps in the extremely tiny dimensions we are producing.
High temperature lead solder is exempted from the requirements of Article (4) of the RoHS directive, **including the use as the interconnect of flip chip packages for very high performance / high reliability packages** due to its excellent thermo-mechanical properties.

Due to the lack of lead-free alternatives for this application, the current RoHS Directive would require manufacturers to switch to a higher lead alternative for all flip chip applications. In this case the additional exemption (see point 10: lead in high melting temperature type solders and any lower melting temperature solder required to be used with high melting temperature solder to complete a viable electrical connection) would be needed.

This request for a new exemption would allow the continued use of low lead concentration solder until lead-free alternatives are found and evaluated. It would be counterproductive for the environment to change to high-lead solders within flip chip packages in order to get coverage by the existing exemptions and the clarification to this existing exemption.

Do any restrictions apply to such substitutes?

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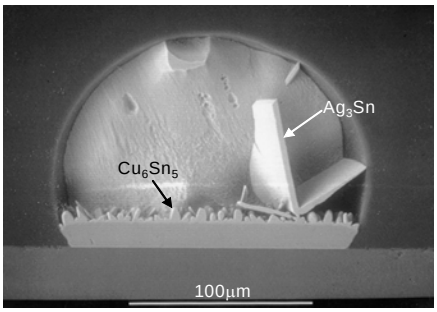
Lead-free solder research is widespread across industry, universities, institutes and national laboratories in all regions of the world. Lead-free solder flip chip interconnections are successfully used today in many applications BUT
our research shows that lead-free substitutes to tiny low temperature tin lead bumps are currently not universally available because:

1. In lead-free solutions, the formation of inter metallic alloys in this tiny bump constitute a high percentage of the joint volume and greatly reduces the resistance to impact (e.g. drop) and thermo-mechanical stresses normally found in the use environment, especially in flexible circuit applications; failure of the joint renders the integrated circuit useless;
2. Lead-free solders with a melting point sufficiently high for mainstream products are much stiffer than eutectic lead-tin solders. This stiffness increases stress on the chip, and can cause premature failure of the chip circuitry.
3. The equipments and materials required for fabricating lead-free bumps are still in the development stage. For example, fluxes for lead-free solder flip chip connections are just now being developed.
4. The industry is still learning the full impact of lead-free solder flip chip interconnect on manufacturability and reliability. For example, it is well known that lead-free solders do not wet (coat) metal terminals as well as lead-tin solders. In order to obtain adequate wetting, new fluxes are being developed. However, the nature of these fluxes impacts other assembly steps and product reliability, and the full extent of the impacts are still being determined.



Undesirable intermetallic alloys make up a significant portion of the experimental lead-free solder bump. Current technologies for the connection between the package and the PWB will not work for interconnect bumps with small dimensions.

A variety of reliability problems have surfaced and no broadly applicable reliable alternative has been identified. To ensure no disruptions in flip chip applications, it is critical to provide a new narrow exemption for low temperature lead-containing solder for these tiny internal connections.

What are the cost and benefits and advantages and disadvantages of such substitutes?

As indicated above there are no lead free substitutes available for the specific applications (tiny dimensions of interconnect bumps).

Time frame for finding potential substitutes:
The ITRS (International Technology Roadmap for Semiconductors) provides an industry identification/assessment of future technical challenges. Alternatives to flip chip connection may be optical interconnects or bump less area arrays (direct copper to copper bonding). These solutions may find their way into products by the end of the decade, but their use will be limited to certain niche applications until the cost is reduced. In the meantime, international chip makers are in active development and are seeking lead-free alternatives to eutectic Pb Sn solders at high speed.