

Nanomagnetic systems for memories & logics

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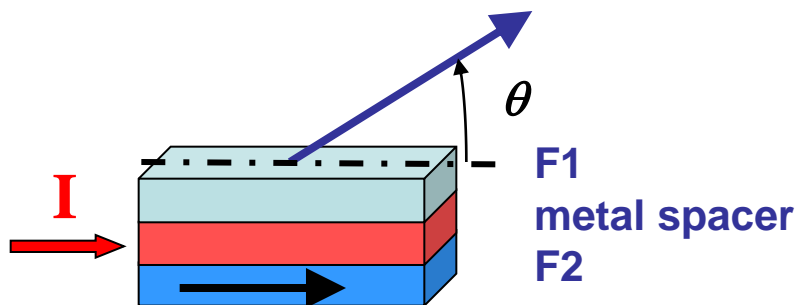


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ANR
NanoINNOV
SPIN

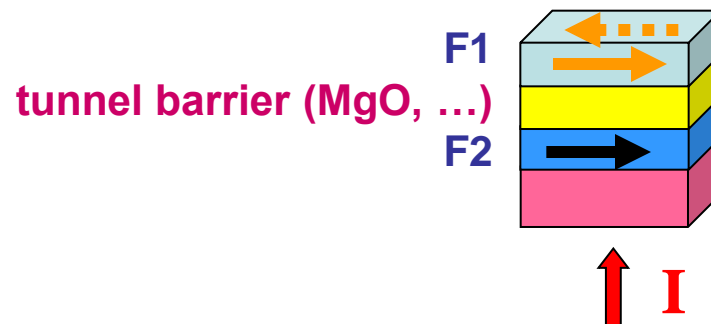
Spin valve (1988-91)



$\Delta R/R \uparrow \uparrow \sim 6 \text{ à } 20 \%$
low R

$$R = R_0 - \Delta R/2 \cos(\theta)$$

Magnetic tunnel junction (1995)



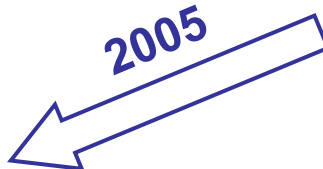
$\Delta R/R \uparrow \uparrow > 1000 \%$
(device: 100-200%)
high R (RA ~ 3-30 $\Omega\mu\text{m}^2$)

1997



High sensitivity sensors:
→ hard disk heads

2005



Non volatile, variable R nanopillar:
→ magnetic M-RAM (Everspin)

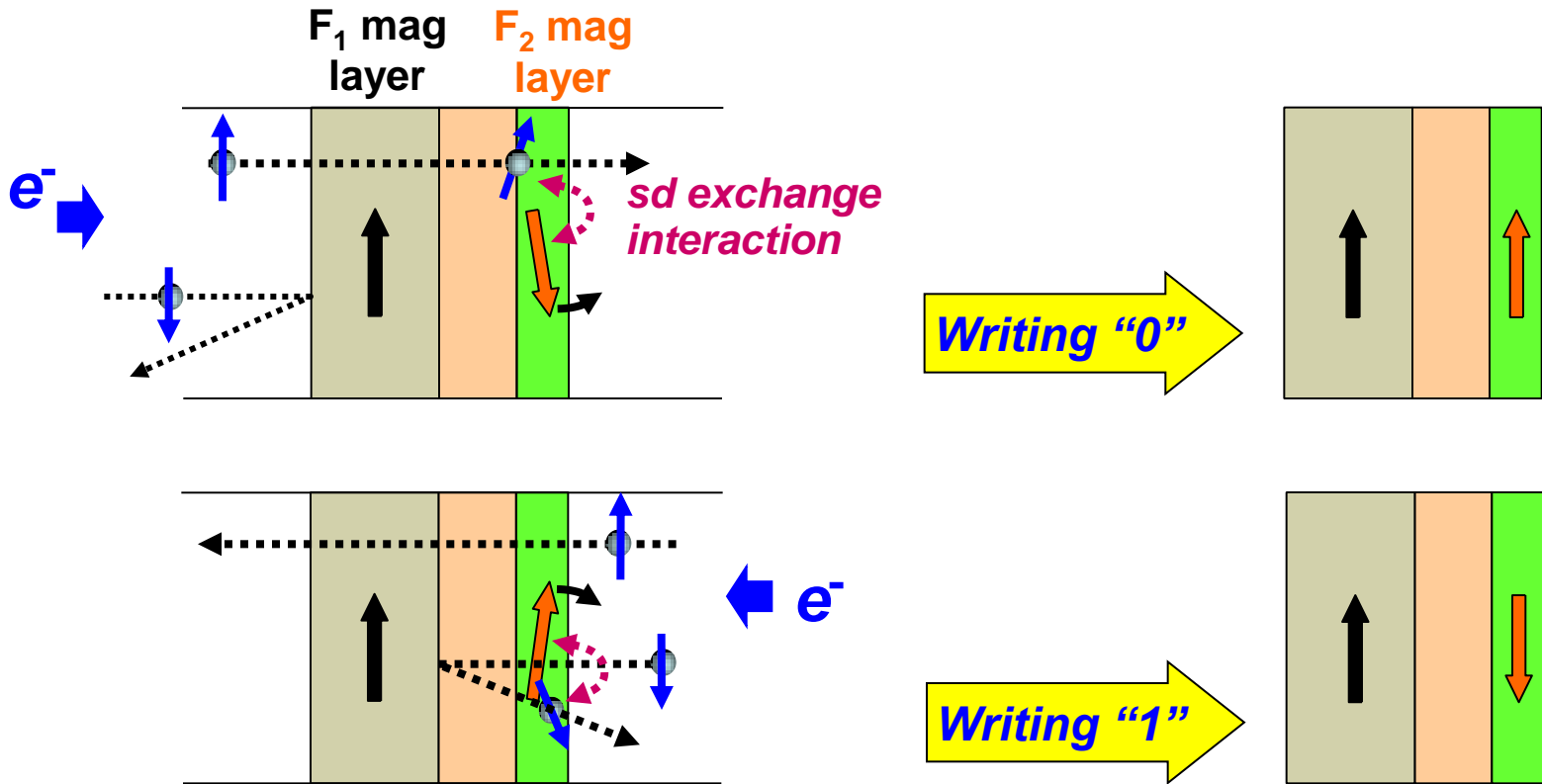
2006



Writing: Spin Transfer Torque switching

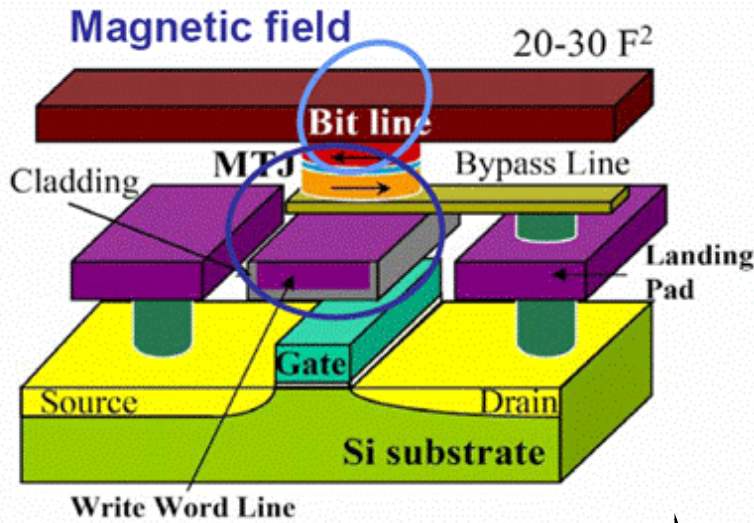
J. C. Slonczewski, JMMM 159, L1 (1996)

exchange interaction between the spin of conduction electrons and M

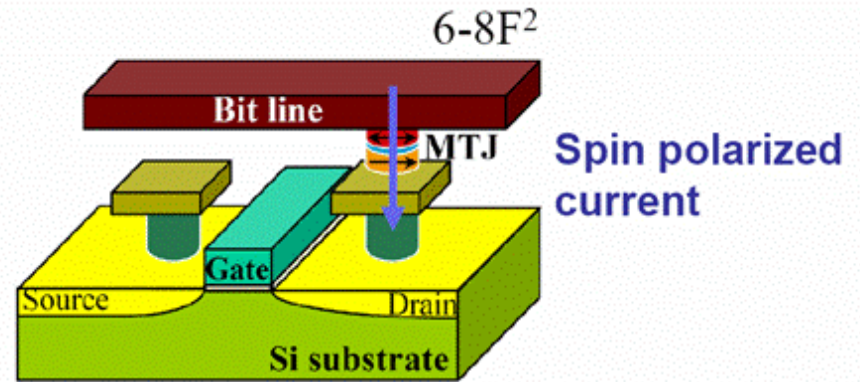


writing by a current density \rightarrow ~scalable

From conventional MRAM... to "spin transfer" STT-MRAM



Freescales's MRAM (2006)



Demo chips of « Spin »-RAM:
SONY, IEDM Dec. 2005
HITACHI, ISSCC March 2007)

- **simple "integrated" architecture, above CMOS technology,**
- **"high" density (<math><10 F^2</math>), potential for downscaling down to 20nm**
- **"fast" (10-30 ns) M-RAM: main advantage of M-RAM versus other NVM RAM....)**

• but still : more costly to fabricate (magnetic back end) and much less dense than Flash (soon 1.3 F² / bit !!!)

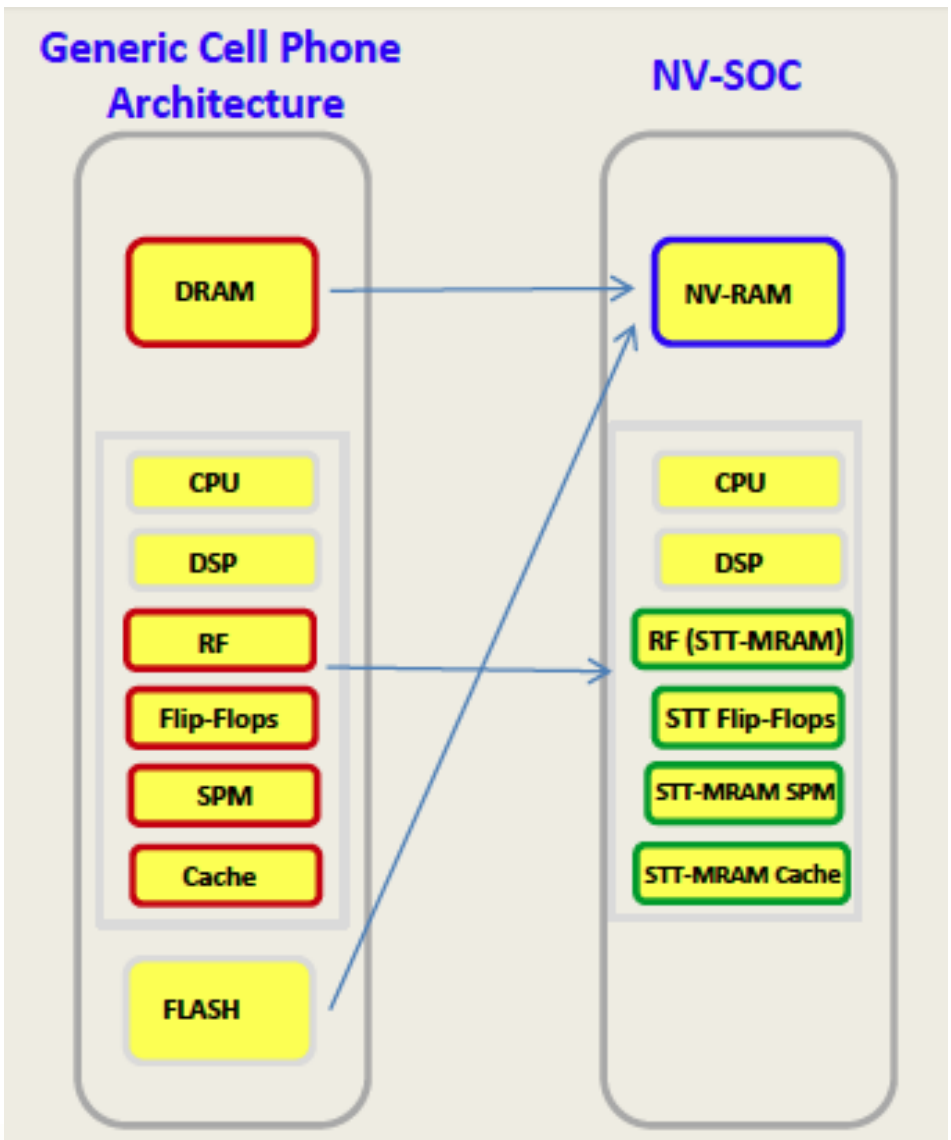


Spin-RAM specifications “to be achieved”

	Products / Demos	Predicted	Position vs CMOS	
Cell size	20 – 80 F ²	~ 10 F ²	>> NAND ≈ DRAM << SRAM	😊
Technology	Above IC		→ embedded NVM	😊
Speed	< 40 ns (2.7 ns)	≤ ns ?	> DRAM ~SRAM, μP	😊
Endurance	10 ¹⁵	~ infinite	>> NAND	😊
Non volatility	> 10 years			😊
Scalability	45 nm	< 20 nm ?	???	↓

R&D 2010 : - potential for DRAM replacement,
- embedded memory,
- standalone for niche applications

Example of STT-RAM impact in SoC

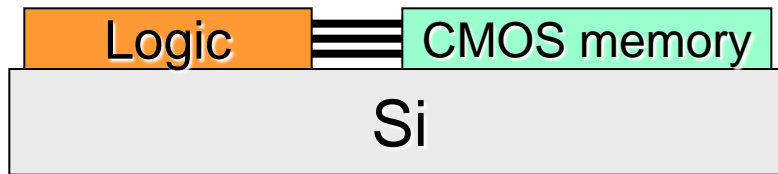


S.H. Kang, Qualcomm,
NVM Workshop, UCSD,
April 11-13 (2010)

45nm CMOS, Logic compatible e-STTRAM produced by Qualcomm/TSMC (IEDM 2009)

- Many companies are scheduling e-MRAM powered MCU :
- Renesas (2012)
 - Qualcomm/TSMC
 - Grandis/NEC/Hynix
 - CROCUS
 - ...

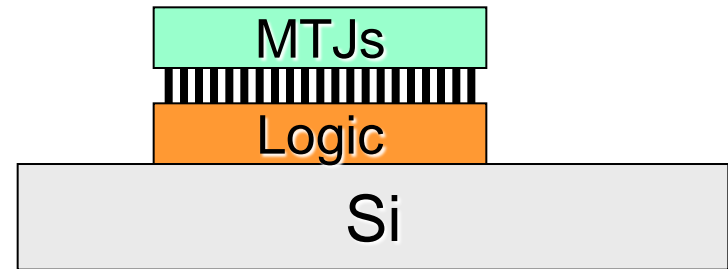
With CMOS technology only:



Slow communication between logic and memory

- **long interconnections**
- complexity of interconnecting paths
- larger occupancy on wafer
- **large static dissipation**
- + general trend towards programmable memory (FPGA, ...)

With hybrid CMOS/magnetic:



Fast communication between logic and memory

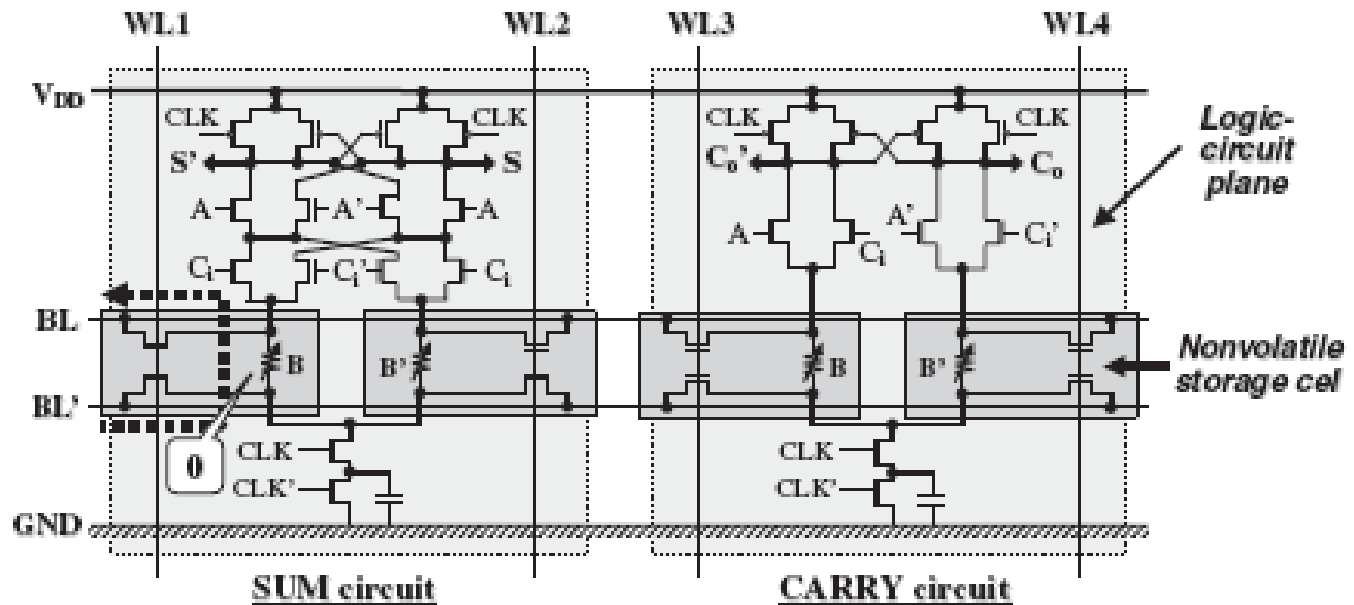
- **numerous short vias**
- simpler interconnecting paths
- Smaller occupancy on wafer
- **instant on/off**
- **extended possibilities for programming and reconfiguration**

New paradigm for architecture of complex electronic circuits (microprocessors...)

Fabrication of a Nonvolatile Full Adder Based on Logic-in-Memory Architecture Using Magnetic Tunnel Junctions

Shoun Matsunaga, Jun Hayakawa¹, Shoji Ikeda², Katsuya Miura^{1,2}, Haruhiro Hasegawa², Tetsuo Endoh³, Hideo Ohno², and Takahiro Hanyu*

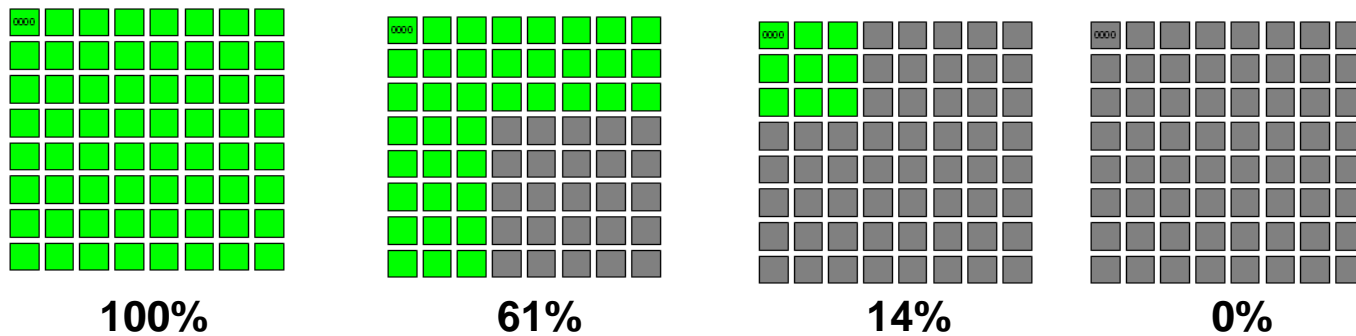
(a)



Low standby Power Programmable logic devices

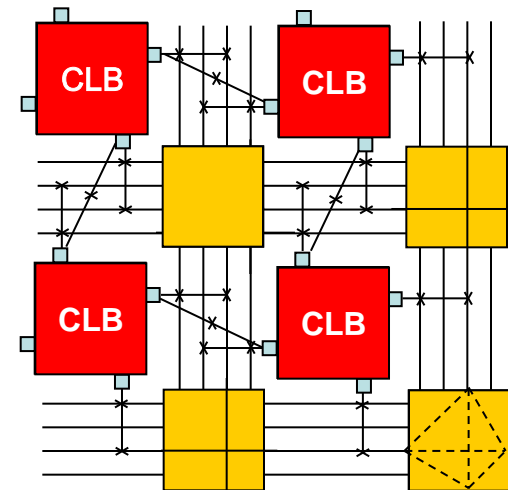
➔ Non volatile, multi-core logic:
 ➔ are powered only the core that need to operate
 ➔ others preserve state and start « instantly » when powered on

■ Active ■ Inactive



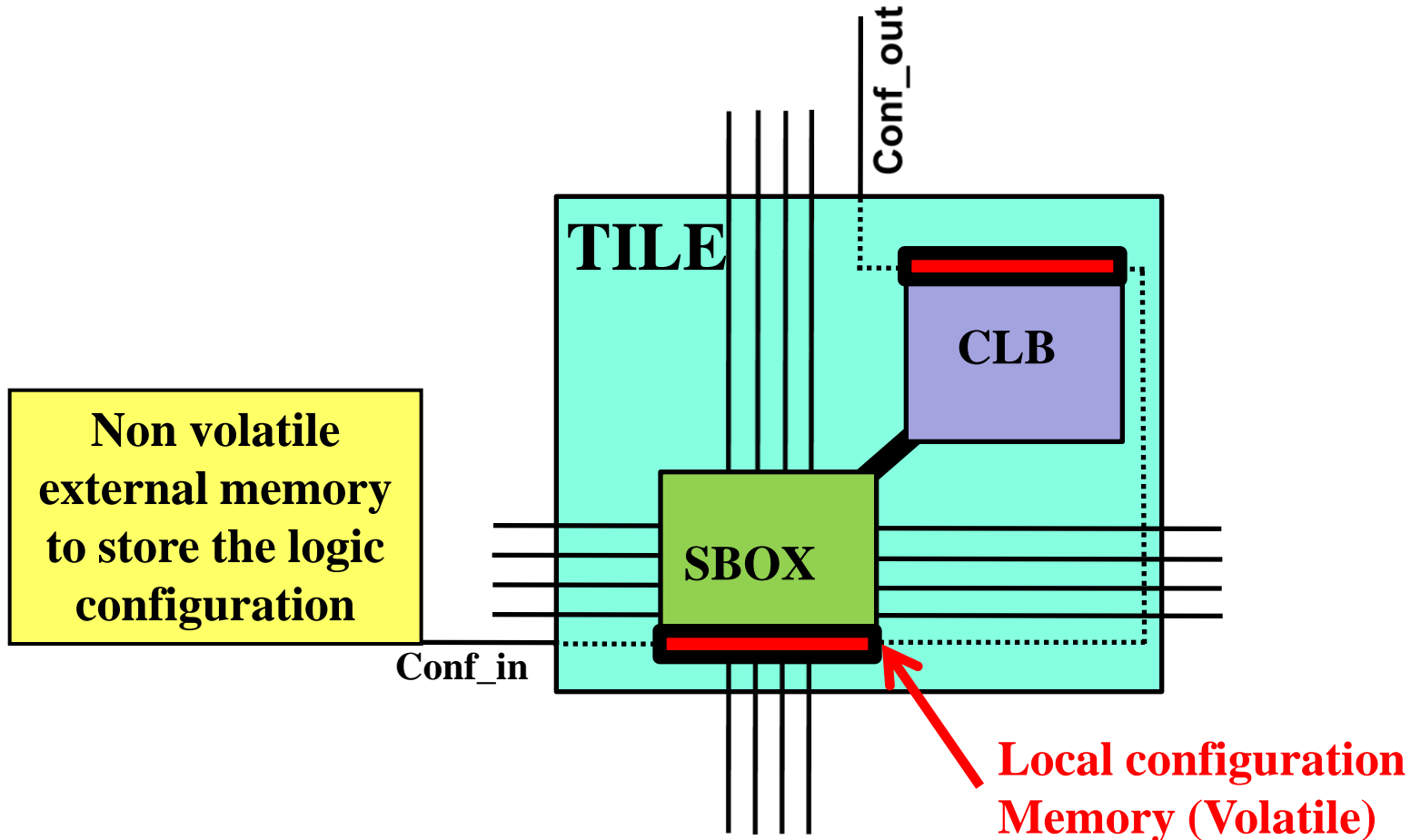
➔ Towards a magnetic FPGA

“switches” and “logic blocs” (CLB) are made:
 ➔ non volatile
 ➔ programmable
 by Spin- MRAM elements



Configuration Memory of a e-FPGA

**L. Torrès,
Y. Guilleminet
L. Rougé**

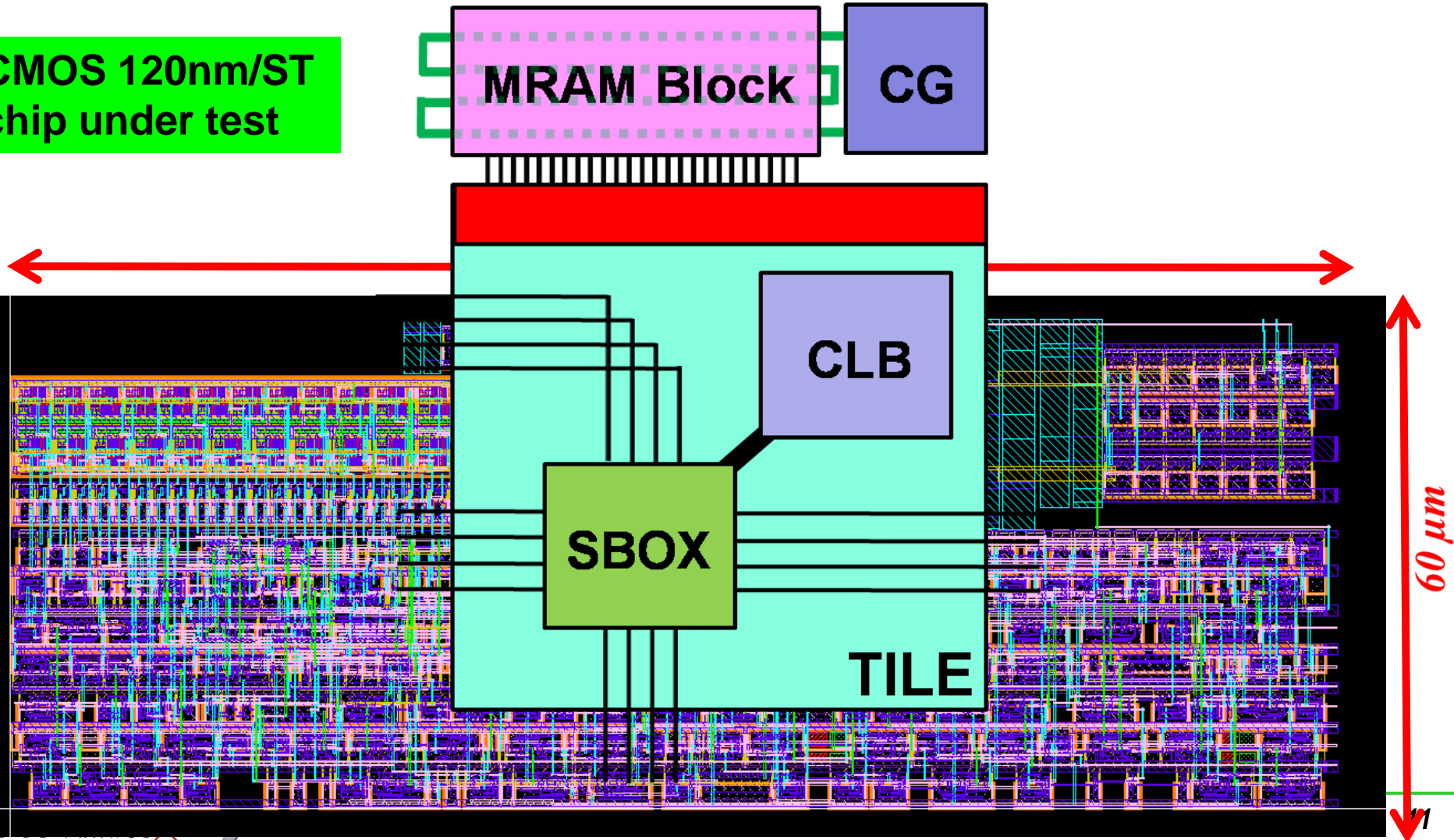




**L. Torrès,
Y. Guilleminet
L. Rougé**

*Thermally assisted
TA- MRAM (CROCUS)*

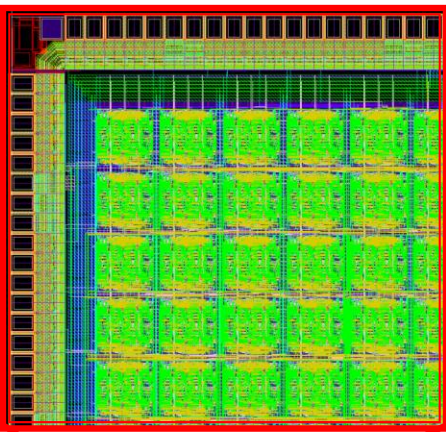
**CMOS 120nm/ST
chip under test**



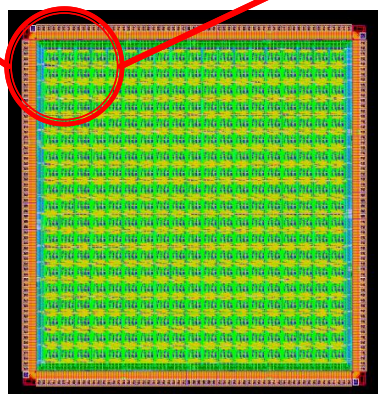


L. Torrès,
Y. Guilleminet
L. Rougé

Above IC magnetic technology at LETI/Grenoble on 120nm CMOS from ST/Crolles



mtile



4504 μ m

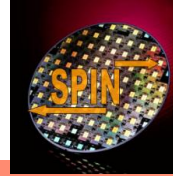
4504 μ m

# LUT 4	1444
# TILES	361 (19x19)
# Sequential elements	1444
# of MTJs	187 720
# of Transistors	$9 \cdot 10^6$
Silicon Area	21mm ²
MRAM Reconfiguration Tile Energy	9 nJ
MRAM Restoration Tile Energy	25,5 pJ
Clock Frequency	100 MHz
Full configuration time	72us + 93K Clock cycles
Tile reconfiguration	200ns + 260 Clock cycles
# Input/Output	76 Input / 76 Output

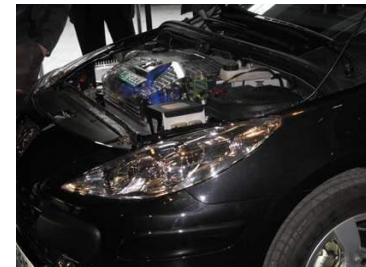
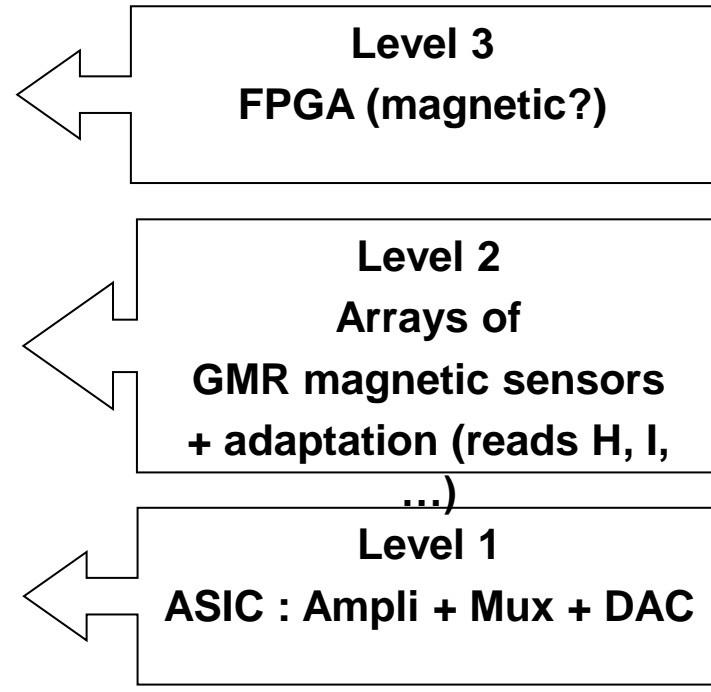
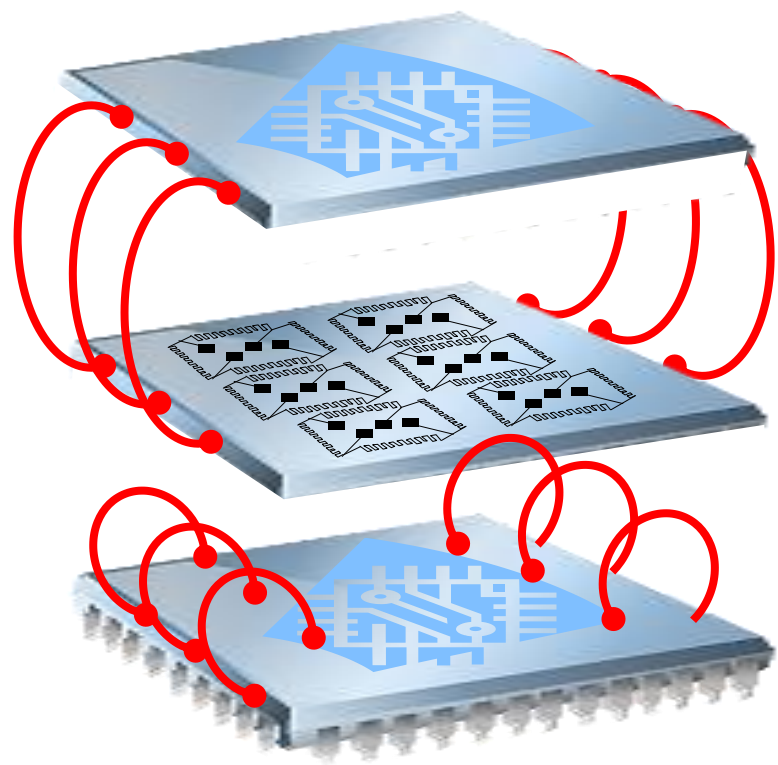
Tâches à effectuer

- Design Kit
- Magnetic Design
- Conception circuit logique
- Layout
- Fonderie Logique
- Dev matériau MRAM
- Dev techno MRAM 120nm
- Fonderie techno MRAM
- Test final





Intelligent chip for monitoring fuel cells or batteries for electric cars...



**Possible:
GMR array
Above IC**

and the scheme can be extended to many applications: health monitoring, chips monitoring, medical imaging, biochips, ...

- with the help of 3 SMEs/Startup:
 - 3DPlus (packaging)
 - CROCUS Technology (MRAM)
 - MENTA (e-FPGA design)

we have tried to close the “Innovation gap” as much as possible by providing demonstrators, expertise and tools (R&D magnetic fab line, Design Kit, ...)

- **involvement of academic nano-scientists in Architecture Design problems** was key issue for arriving there: multidisciplinary collective effort
- up to 10 patents will be filed in a 1.5 year span: some IP is “in house”
- many markets don't require advanced CMOS technology : many fab in EU

Next research :

- core IP development for embedded e-MFPGA
- radiation hard FPGA for space and airplane
- neuro-inspired magnetic logic
- ...

